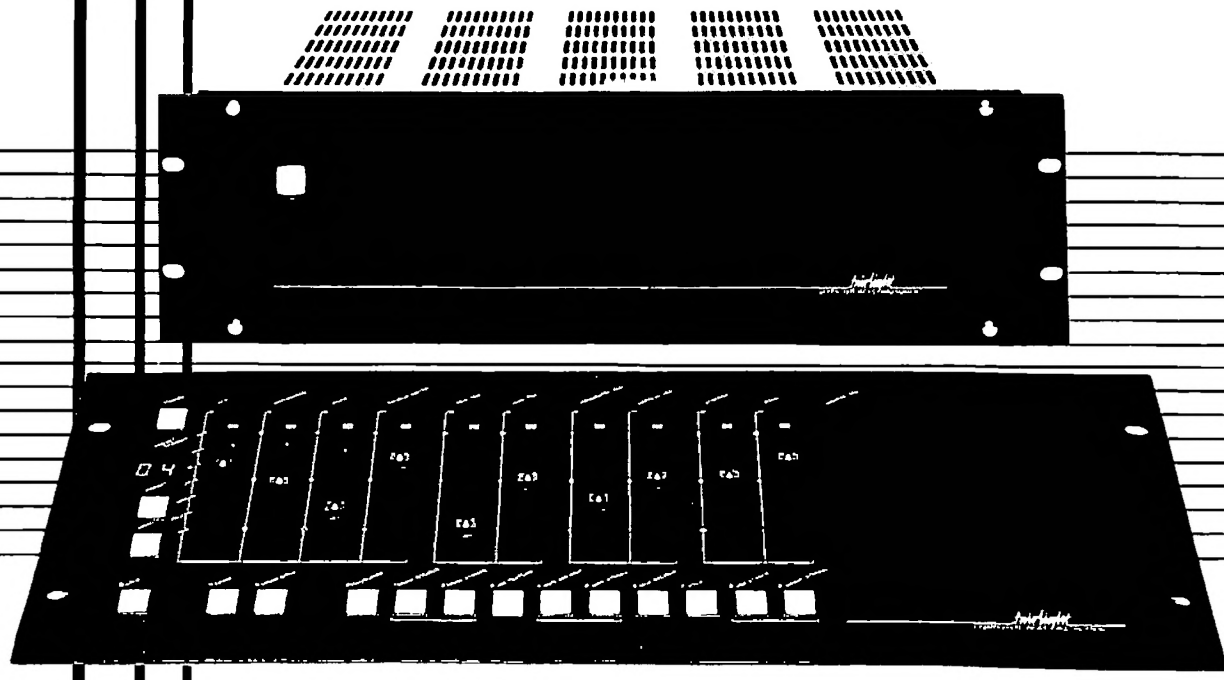
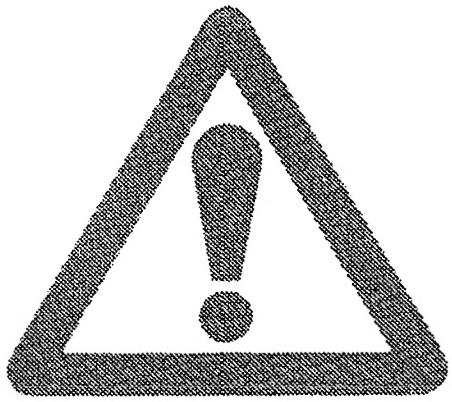


CVI

COMPUTER VIDEO INSTRUMENT

SERVICE MANUAL

FAIRLIGHT JUNE 1985



**These service instructions are for use by qualified personnel.
If nontechnical CVI owners suspect that the unit has degraded,
or that some functions are not working,
perform the self diagnostic tests (Video menu 9) first
then report error messages to your distributor.**

Fairlight Pty Ltd., 15 Boundary Street, Rushcutters Bay, N.S.W 2011
Sydney, Australia
Phone: (02) 331 6333, Telex: 27998 'FAIRLT'

System Overview 1

CONTENTS

Video standard:	NTSC or PAL compatible (note 1).
Field store:	256 x 256 pixels, 14 bit planes, 4096 colours (note 2).
Memory:	128 Kbytes RAM, 32 Kbytes ROM.
Processor:	2MHz 6809.
Communications:	RS232C port (300 - 19200 baud). Internal functions can be accessed and controlled by ASCII codes.
Expansion:	Processor expansion bus, Digital video cascade in and out.
Composite video inputs:	x2, 1Vp-p, loop through
RGB inputs:	x2, 0.7Vp-p, loop through
Composite video output:	1Vp-p, 75 ohms (note 3).
RGB output:	0.7Vp-p, 75 ohms.
Stencil (key/matte) in:	0.7V dc slicing level.
Stencil out:	2Vp-p, 75 ohms.
Resolution:	> 300 lines (composite in - composite out). 256 pixels per line (field store).
Delay:	1300 ns (composite in - composite out).
Subcarrier:	Internally generated or external input (loop through) 1V to 4V p -p. 0 - 360 degree phase control.
Synchronization:	Internally generated for stand-alone use. Auto external sync to composite video 1 input.
Termination:	Switchable 75 ohm termination inbuilt on all video inputs.
Video connections:	Full complement of BNC connectors (26).
Audio input:	Internal mic, external mic or line.
Power:	40W (100 - 120 or 200 - 240 volts).
Dimensions and Weight:	Control panel: 428(W)x178(H)x25(D) mm. Multicore cable between control panel and electronics unit. Standard length: 2m optional: 5, 10 or 20m. Standard EIA rack size, 4 units. 1Kg. Remote electronics unit: 482(W)x133(H)x270(D) mm. Standard EIA rack size, 3 units. 6kg.

Please note:

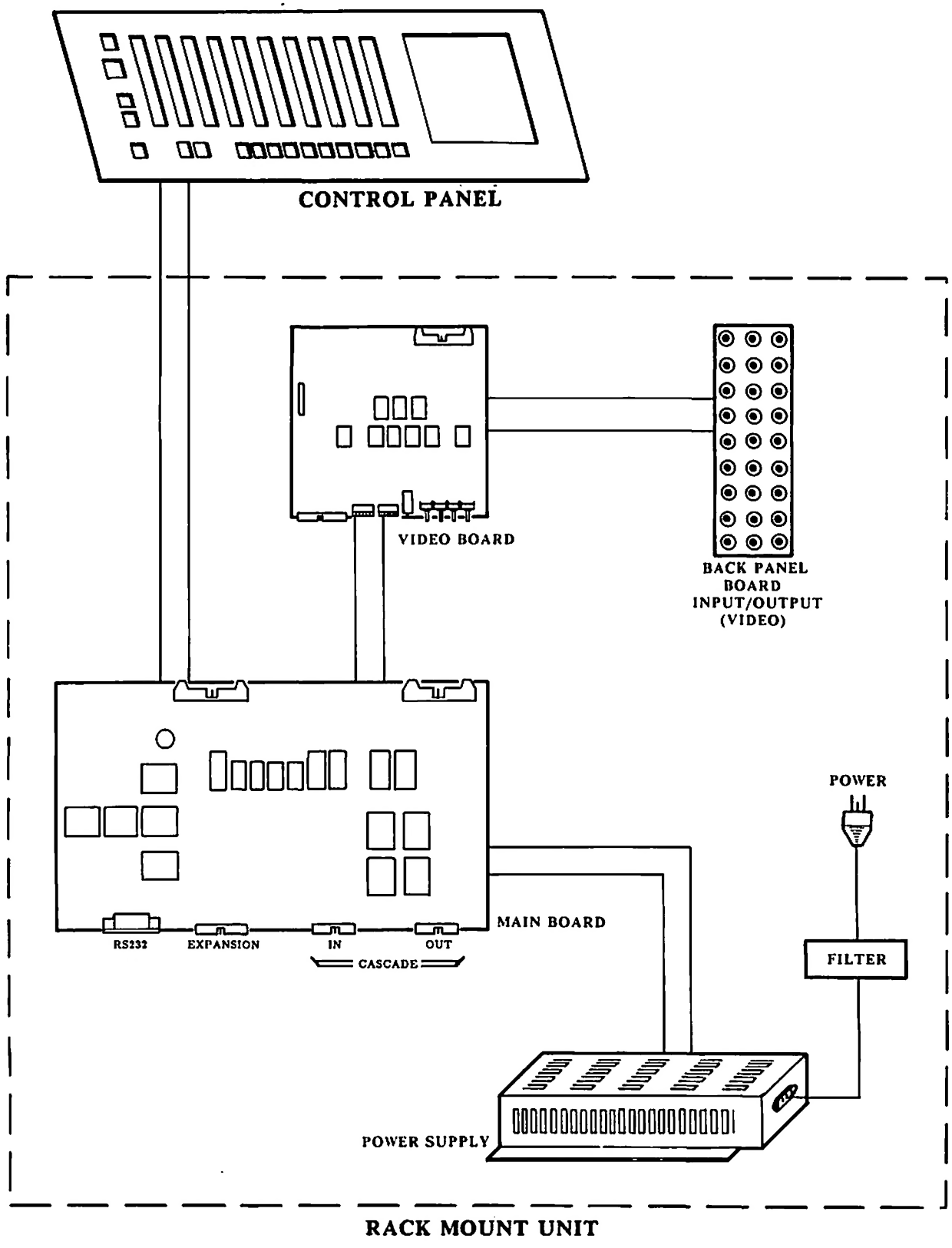
(1) In PAL systems field store displays only 256 lines. This will normally be visible as 3 to 5 black lines at the top and bottom of the digitally stored picture, depending on the monitor vertical scanning adjustments.

(2) CVI will not squeeze or zoom LIVE images.

(3) If used in a studio installation where the CVI output is to be mixed with other sources, or where broadcast style output is required, an external PAL/NTSC coder and SPG should be used.

* These specifications are subject to change and are presented as a guide only.

CVI OVERVIEW BLOCK DIAGRAM



The Computer Video Instrument is a computer controlled field store. It is compatible with either PAL or NTSC systems and can be used with most video sources including cameras, VTR's and VCR's. Two genlocked RGB or composite video inputs can be used. Composite and RGB outputs are provided.

The video signal is processed initially on the Video Board before being sent to the Main Board for switching/mixing or digital processing. The signal is then returned to the Video Board for further processing before being output.

The system uses separated red, green and blue colour components for processing by the computer instead of luminance and colour difference components used in other digital video systems. This reduces the amount of computation necessary. RGB component signals are therefore used throughout the system in both analog and digital form.

The system comprises five main sections: Video Board, Main Board, BNC Connector Board, Control Panel and Power Supply.

The CVI is housed in a standard 19" rack-mounting case. The Video Board and Power Supply Assembly are mounted on the top of the central tray which slides out for servicing and adjustment. The Main Board is mounted on the underside of this tray. The BNC Connector Board is mounted on the back panel. The Control Panel is housed in a separate rack-mounting assembly.

Separate PAL and NTSC versions of the Video Board are available. The Main Board, Control Panel, BNC Connector Board and Power Supply are used for both TV standards.

The functions of each are now described. Refer to the block diagram.

Video Board

This card contains the composite video decoders, sync separator, colour subcarrier oscillator, encoder, delay lines, buffers, RGB multiplexers and audio filters. It connects to the Main Board via a forty way ribbon cable.

The main functions performed on this card are:

- decoding the input composite video signals to red, green and blue analog signals.
- switching these signals to the selected analog and digital paths.
- generating the subcarrier signal to be used by the Main Board as a reference frequency.
- generating horizontal and vertical sync signals from the incoming video signals.
- generating the audio control signals from the internal microphone or external audio input.
- encoding the final analog RGB signals from the Main Board into a composite video signal.

Main Board

This card contains the microcomputer, field store, analog-to-digital and digital-to-analog converters, chroma-key circuitry, control, timing and interface circuitry.

The main functions performed on this card are:

- conversion of analog RGB signals to digital signals.
- generating the internal and chroma-key stencils.
- generating the timing and control signals for the whole system.
- communicating with external devices via the RS232 port.
- monitoring the status of the control panel.
- displaying and updating the menu displays.
- storing a field of digitised video information.
- processing the digital signals for such effects as colorisation, freeze, zoom, pan, stretch, mirror, etc.
- generating the final analog RGB signals from the digital and analog RGB signals.

Control Panel

This unit contains the switches, control sliders, graphics pad and preset display. It connects to the Main Board via a forty way ribbon cable upto twenty metres in length.

The main functions performed by the Control Panel are:

- generating the control signals from the switches and sliders.
- deriving position information from the graphics pad.
- displaying the preset number.
- indicating the status of various functions on the switch LEDs and buzzer.

BNC Connector Board

This board contains all the input and output connectors. It connects to the Video Board via a forty way ribbon cable.

Power Supply

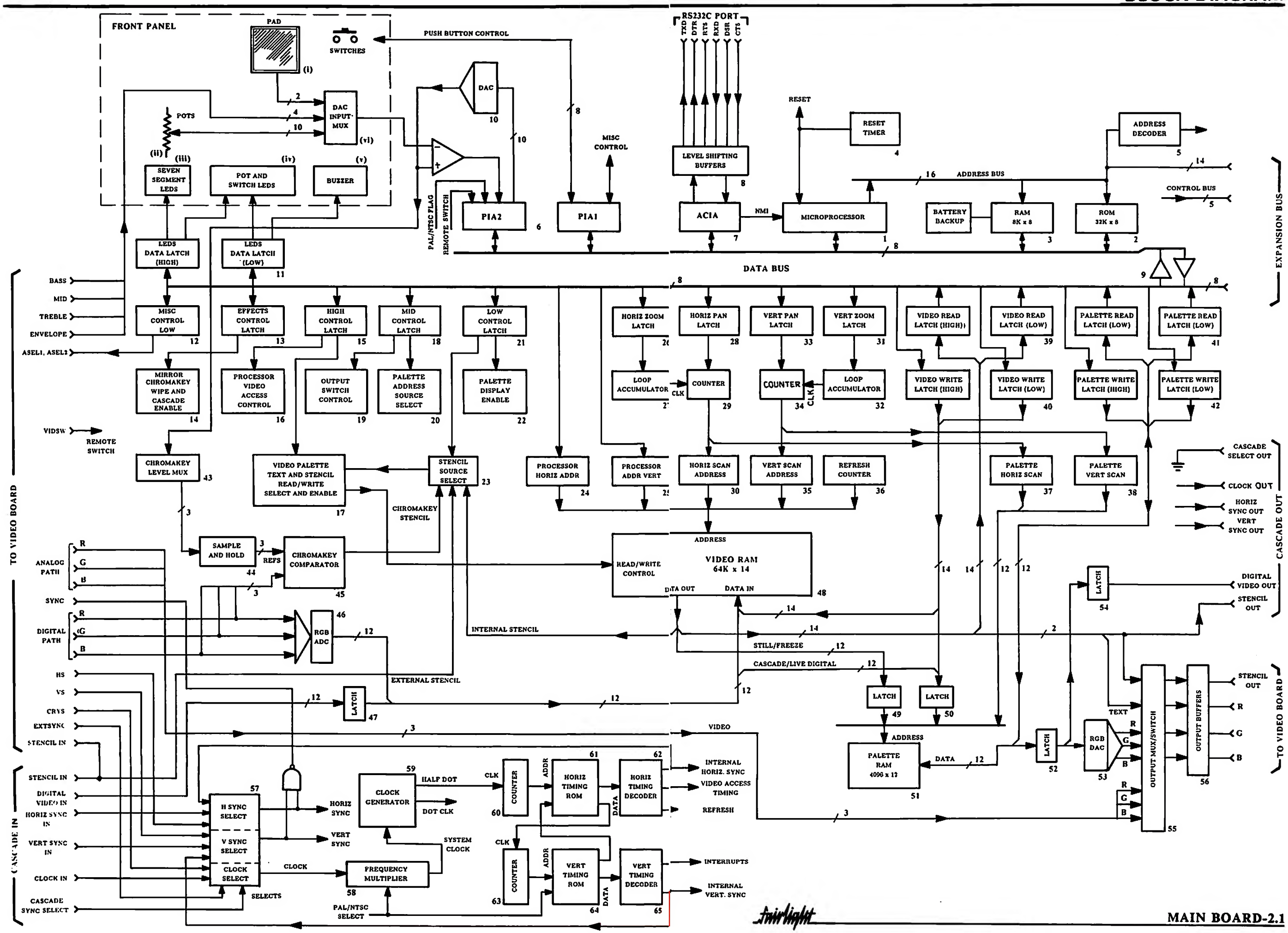
This unit consists of a switch mode power supply unit, on/off switch and mains socket and filter. It provides the +12v, +5v, -12v and 0V supply rails required by the CVI. It connects to the Main Board via a fourteen way ribbon cable.

Main Board Control Board

2

CONTENTS

BLOCK DIAGRAM



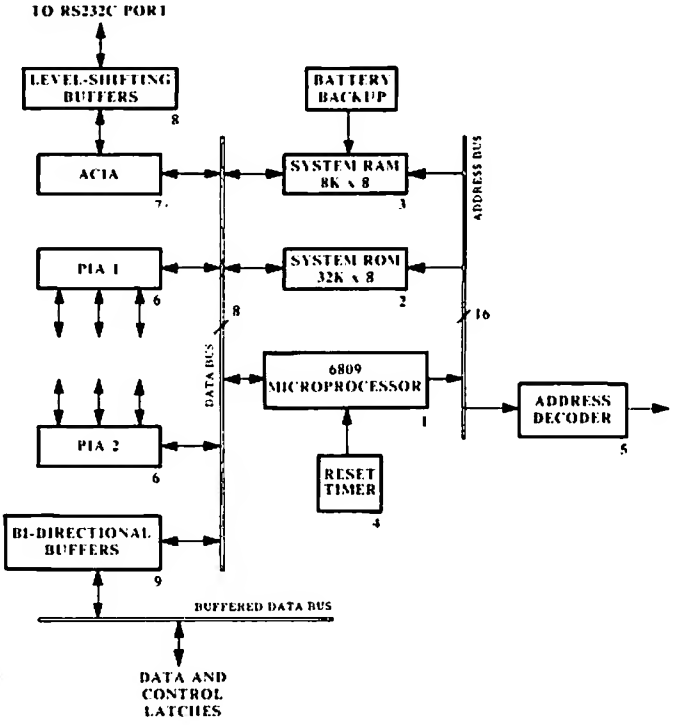
Fairlight

MAIN BOARD-2.1

NOTE: For easy reference, the numbers preceeding each paragraph coincide with the block under description on Main Board Block Diagram - Page 2.1.

The numbers in brackets [ ] refer to the ICs under description. See overlay Page 2.4.

The numbers in parenthesis ( ) refer to Circuit Diagrams No CVI 01, Sheets 1-10, Page 2.5-2.5.9



1. 6809 microprocessor runs at 2MHz, asynchronously to the video timing. The processor controls 32K of ROM, 8K of static RAM, two PIA's and one ACIA, as well as four read-only and seventeen write-only latches on a buffered data bus. Processor RAM or ROM may be expanded by up to 16K by using the expansion port.

IRQ interrupts are generated once per frame to initiate hardware configuration activity. All the control latches are set during the IRQ interrupt. FIRQ interrupts are generated four times per frame to update the control-panel LEDs without flicker. NMI interrupts are generated when a character is received or transmitted from the serial port (7). Further synchronisation to the video timing is achieved by polling PIA inputs as required. [A7 (CVI01 Sheet 1)]

2. System ROM is 32Kx8. The two 16K chips are removable to accommodate software upgrades. [B7,C7 (CVI01 Sheet 1)]

3. System RAM is 8Kx8 of static RAM. Battery backup retains the preset and sequencer data on power-down. [D7 (CVI01 Sheet 1)]

4. Reset timer provides the power-up reset pulse to the processor and to much of the digital circuitry. [F19 (CVI01 Sheet 1)]

5. Address decoder decodes the address bus into enable signals for each of the processor peripherals, for the expansion bus, and for each of the twentyone processor-accessible 8-bit latches. [E17,E18,E19,E20,E21 (CVI01 Sheet 6)]

6. Parallel interfaces control the analog input multiplexer on the control-panel, the chromakey level multiplexer and control-panel switch decoding. The PIA's also provide software access to hardware timing signals and control the IRQ and FIRQ interrupts to the processor. [F12,F16 (CVI01 Sheet 1)]

7. Asynchronous communications interface has programmable baud-rate with timing generated from an external crystal. It is programmed for RS232C communications. The ACIA causes NMI interrupts to the processor on data transfer. [A4 (CVI01 Sheet 1)]

8. Data buffers convert the TTL ACIA signals to +/-12V line signals and vice versa. [A1,A2 (CVI01 Sheet 1)]

9. Bi-directional buffers isolate the processor data bus from the hardware latches, and provide current-drive capability. [A12 (CVI01 Sheet 1)]

10. Analog-to-digital converter is implemented with a 10-bit DAC, a comparator and a successive-approximation algorithm. An analog-to-digital conversion is performed only when an input has changed since the previous reading. The DAC also sets the chromakey levels. [F21,G22 (CVI01 Sheet 9)]

11. **LEDs data latch** (16-bit) controls the data and multiplexing sequence for the control-panel LEDs and the buzzer. Four transistor drivers provide current drive. [F8,F9 (CVI01 Sheet 5)

12. **Miscellaneous control latch** (8-bit) controls the multiplexer that selects the video source for each of the analog and digital paths. The multiplexer is located on the video board. The latch also enables extended vertical blanking. [C29 (CVI01 Sheet 7)]

13. **Effects control latch** (8-bit) enables mirror, wipe, chromakey and cascade effects. The bits of the latch each enable or control dedicated hardware logic. [C15 (CVI01 Sheet 7)]

14. **Effects control** is performed by the effects control latch (13).

Horizontal and vertical mirrors are created by enabling counting-direction reversal in the video-address counters (29,34).

Horizontal and vertical wipes are created by enabling carry-out from the video-address counters to swap between the still and live digital image sources.

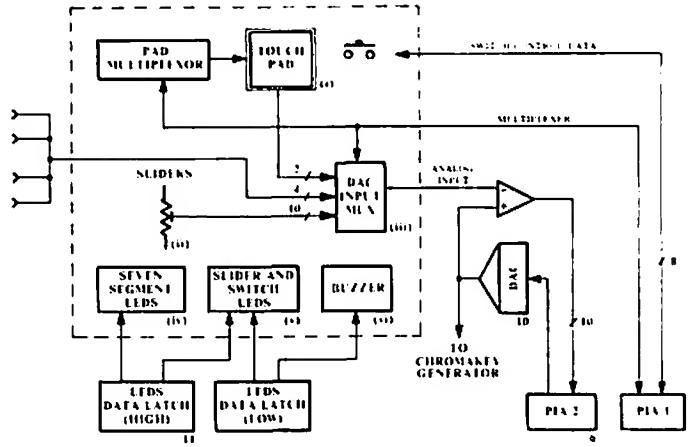
Cascade of a digital image from another CVI is enabled by selecting data from the cascade input latch (47) instead of from the ADC (46).

Chromakey-type selection (blue or luminance) is made by altering the logical combinations of the chromakey comparator outputs (45). [(CVI01 Sheets 3 & 7)]

15. **High control latch** (8-bit) stores the processor read/write control signals for the video, stencil, text and palette memories (48,51). [C14 (CVI01 Sheet 7)]

16. **Processor video access control:** Processor access to the video and palette memories is restricted by the horizontal timing generator (62) to once in each video line. A hardware status flag is set when a control word is written to the high control latch (15). The flag is subsequently cleared after the data transfer is completed in the next processor access cycle. The processor reads the flag through PIA1, and hence avoids overwriting unwritten data or reading old data. [E12 (CVI01 Sheet 7)]

17. **Video and palette RAM read/write control:** The latched signals from the high control latch are used during the processor access cycle to enable the processor data latches (39,40,41,42) and to generate read or write pulses to the



appropriate sections of memory. [D14 (CVI01 Sheet 7)]

18. **Mid control latch** (8-bit) stores control signals which operate the output switch (55), determine whether stored or direct image data addresses the palette, and determine whether incoming image data is written to the video RAM. [C13 (CVI01 Sheet 7)]

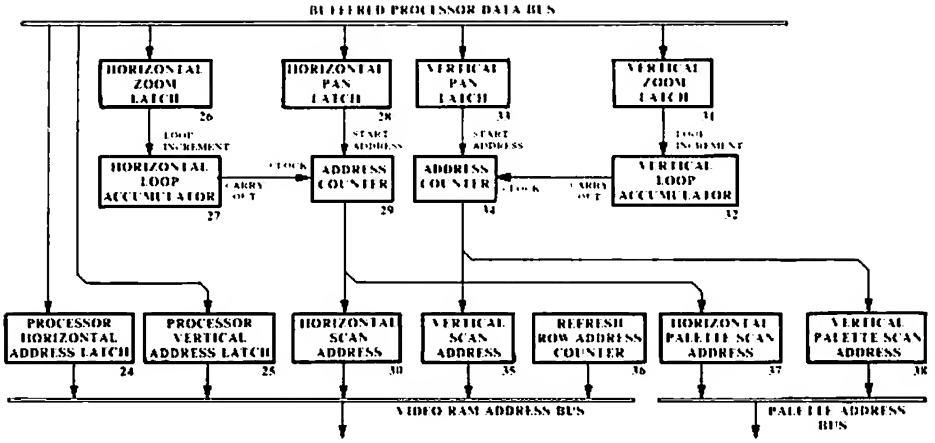
19. **Output switch control:** Four latched bits from the mid control latch are used to select RGB outputs from either the digital or analog path or both for when the stencil is on and for when it is off. The four bits are combined with the stencil to form two control signals to the output switch (55). [B13 (CVI01 Sheet 7)]

20. **Palette address source select** hardware determines whether the palette address data (and hence the output of the digital path) is taken from the video RAM (still or freeze) or directly from the digital input (live digital or cascade). [D9 (CVI01 Sheet 7)]

21. **Low control latch** (8-bit) stores data that determines which stencil is to be used and whether the stencil, text page or the palette is displayed. [C16 (CVI01 Sheet 7)]

22. **Palette display enable** logic allows the video address counters (29,34) to address the palette via the palette scan latches (37,38). This causes the output of the digital path to be an ordered display of the palette RAM that can respond to pan and zoom. [(CVI01 Sheet 7)]

23. **Stencil source select** uses three bits from the low control latch to select the active stencil from the internal, external and chromakey stencils. [E14 (CVI01 Sheet 7)]



24. Processor horizontal address latch (8-bit) contains the high-order address during a video RAM access by the processor. Data is transferred through the video read or write latches (39 or 40) under the control of the processor video access control logic (16). [C19 (CVI01 Sheet 3)]

25. Processor vertical address latch (8-bit) contains the low-order address during a video RAM access by the processor. [C20 (CVI01 Sheet 3)]

26. Horizontal zoom latch (8-bit) holds the input data for the loop accumulator (27) that controls horizontal pixel zooming. [B12 (CVI01 Sheet 5)]

27. Horizontal loop accumulator (8-bit) increments once each pixel period by the value stored in the horizontal zoom latch. The carry-out from the accumulator enables clocking of the horizontal video address counter. Hence a small value in the zoom latch causes one pixel to be displayed many times, resulting in stretch. [B9,B10,B11 (CVI01 Sheet 5)]

28. Horizontal pan latch (8-bit) holds the start address for the horizontal video address counter (29). In slide mode the start address is increased each frame. [C17 (CVI01 Sheet 3)]

29. Horizontal address counter increments through horizontal video addresses at a rate determined by the horizontal zoom logic (26,27). Counting begins at the address stored in the horizontal pan latch and continues to the end of the video line. The carry-out is used to determine the position of horizontal mirrors and wipes when they are activated. [A15,A16,A17,A18 (CVI01 Sheet 3)]

30. Horizontal scan address latch (8-bit) holds the address from the horizontal address counter. [A19 (CVI01 Sheet 3)]

31. Vertical zoom latch (8-bit) holds the input data for the loop accumulator (32) that controls vertical pixel zooming. [C12 (CVI01 Sheet 5)]

32. Vertical loop accumulator (8-bit) increments once each line period by the value stored in the vertical zoom latch. The carry-out from the accumulator enables clocking of the vertical video address counter. [C9,C10,C11 (CVI01 Sheet 5)]

33. Vertical pan latch (8-bit) holds the start address for the vertical video address counter (34). In slide mode the start address is increased each frame. [C18 (CVI01 Sheet 3)]

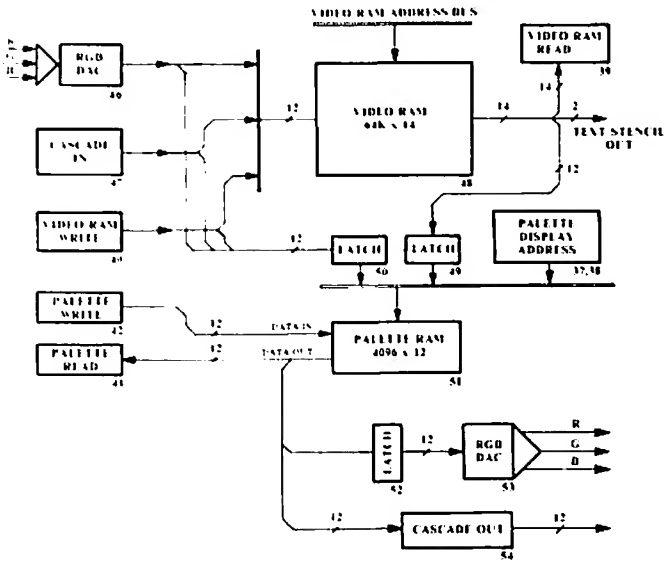
34. Vertical address counter increments through vertical video addresses at a rate determined by the vertical zoom logic (31,32). Counting begins at the address stored in the vertical pan latch and continues to the end of the video field. The carry-out is used to determine the position of vertical mirrors and wipes when they are activated. [A13,A14,B17,B18 (CVI01 Sheet 3)]

35. Vertical scan address latch (8-bit) holds the address from the vertical address counter. [A20 (CVI01 Sheet 3)]

36. Refresh counter continually refreshes the dynamic video RAM during the horizontal blanking periods by cycling through the row addresses. [B19,B20 (CVI01 Sheet 3)]

37. Palette horizontal scan latch (6-bit) takes addresses from the horizontal pan/zoom counter (29). If the palette display logic (22) enables the latch then the addresses are applied to the palette RAM to give an ordered palette display. [A21 (CVI01 Sheet 3)]

38. Palette vertical scan latch (6-bit) takes addresses from the vertical pan/zoom counter (34). If the palette display logic (22) enables the latch then the addresses are applied to the palette RAM. [A22 (CVI01 Sheet 3)]



39. Video read latch (16-bit) contains the 14 bits of data after a processor read from the video RAM. [C21,C22 (CVI01 Sheet 2)]

40. Video write latch (16-bit) is the write-data latch for the video RAM and the address latch for the palette RAM. The control word written to the high control latch determines which function is required. [C23,C24 (CVI01 Sheet 2)]

41. Palette read latch (16-bit) contains the 12 bits of data after a processor read from the palette RAM. [C27,C28 (CVI01 Sheet 4)]

42. Palette write latch (16-bit) contains the 12-bits of data for a processor write to the palette RAM. [C25,C26 (CVI01 Sheet 4)]

43. Chromakey level multiplexer updates the red, green and blue analog chromakey levels to the three sample-and-hold circuits every field under processor control. The analog levels are supplied from the DAC (10) and the multiplexer is controlled from PIA1. [F23 (CVI01 Sheet 9)]

44. Sample and holds hold the chromakey reference levels set by the processor. [(CVI01 Sheet 9)]

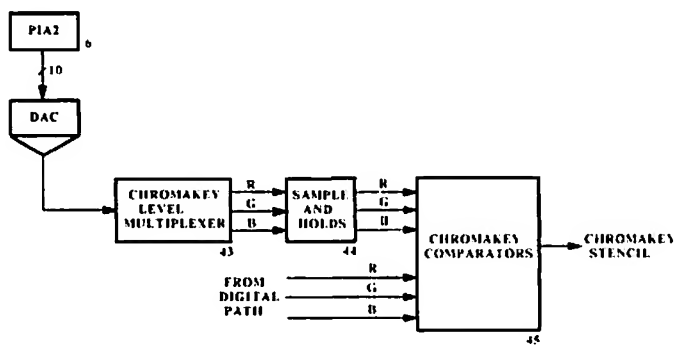
45. Chromakey comparator compares the incoming red, green and blue levels with the chromakey references. The comparator outputs are combined logically with the chromakey-type controls from the effects latch (13) to generate the chromakey stencil. [G24,G25,G26 (CVI01 Sheet 9)]

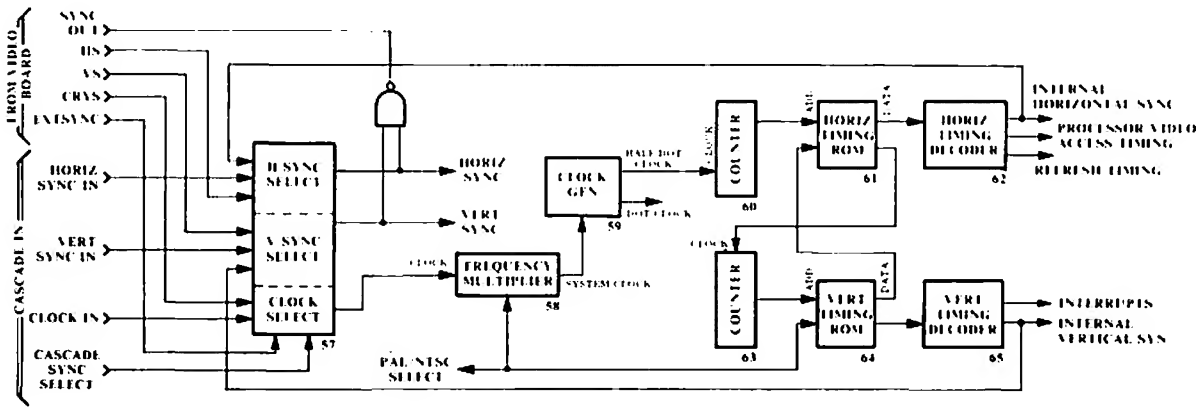
46. RGB digital-to-analog flash converter digitises each of the red, green and blue signals to four bits. The 12-bit output may be stored in the video RAM (still/freeze) or used to address the palette (live digital). [E24,E25,E26 (CVI01 Sheet 9)]

47. Cascade input latch (16-bit) enables image data to be cascaded from another CVI. The latch is enabled via the effects control latch (13). [A23,A24 (CVI01 Sheet 4)]

48. Video RAM is 64Kx14 bits of dynamic RAM. The 64K locations correspond to the 256x256 pixel locations. Each pixel location has 12 bits of colour information, one bit for the stencil information and one bit for the menu page. [D17,D18 ... D29,D30 (CVI01 Sheet 2)]

49. Palette address latch (12-bit) allows direct digital image data or processor data to address the palette RAM. This latch is enabled from the palette-address selection logic (20). [B23,B24 (CVI01 Sheet 4)]





50. Palette address latch (12-bit) allows stored image data from the video RAM (48) to address the palette RAM. This latch is enabled from the palette-address selection logic (20). [B21,B22 (CVI01 Sheet 2)]

51. Palette RAM is 4Kx16 bits of static RAM of which 4Kx12 bits are used. It performs a colour transformation, allowing each colour to be mapped to any other colour. The 12-bit address is pixel colour data from the video RAM or from the direct video inputs. The 12-bit data output is the transformed or colourised value of the addressing colour. Data is written to the palette RAM only by the processor, through the video and palette write latches (40,42). [A25,A27,B25,B27 (CVI01 Sheet 4)]

52. Palette output latch (16-bit) clocks the transformed colour data from the palette RAM to the RGB digital-to-analog converter and to the cascade output. [A28,B28 (CVI01 Sheet 4)]

53. RGB digital-to-analog converter converts the twelve bits of colour information from the digital path back into three analog signals (red, green and blue). [E27,E28,E30 (CVI01 Sheet 10)]

54. Cascade output buffer (16 bit) buffers the digital video outputs to a second CVI. [A29,B29 (CVI01 Sheet 4)]

55. Video output switch combines the digital and analog paths, the stencil and the menu page into the final image format. Each of the red, green and blue outputs is formed by the selective analog addition of the digital path, analog path, stencil and text signals. This enables such functions as menus, show-stencil, video-mix, live digital, still, video, etc. The adder is controlled by the output-switch control logic (19) and by the low control latch (21). [E27,E28,E30 (CVI01 Sheet 10)]

56. Output buffers buffer the output of the video switches. [G27,G28,G30 (CVI01 Sheet 10)]

57. Sync source select circuit selects the source of the system sync signals according to the status of EXTERNAL SYNC and CASCADE SYNC lines. EXTERNAL SYNC is enabled if an input is connected to the CVI Video 1 input. CASCADE SYNC is enabled if an input is connected to the Cascade In port. System sync signals are selected, as appropriate, from the internal syncs (62,65), from the sync derived from the external video signal, or from the cascade syncs. The twice-subcarrier signal is selected either from the clock on the video board or from the cascade input clock. [B3,B4,B5 (CVI01 Sheet 8)]

58. Frequency multiplier uses a phase-locked loop to multiply the twice-subcarrier clock by four for PAL or five for NTSC to give the 35MHz system clock. [F1,F4 (CVI01 Sheet 8)]

59. **Clock generator** uses the 35MHz system clock from the frequency multiplier to generate a number of hardware clocks. The pixel (dot) clock is the system clock divided by 8. [F5 (CVI01 Sheet 8)]

60. **Horizontal timing counter** addresses the horizontal timing ROM sequentially. It is clocked at twice the pixel rate, and is cleared by the system horizontal sync pulse from the sync selector (57). [D1 (CVI01 Sheet 8)]

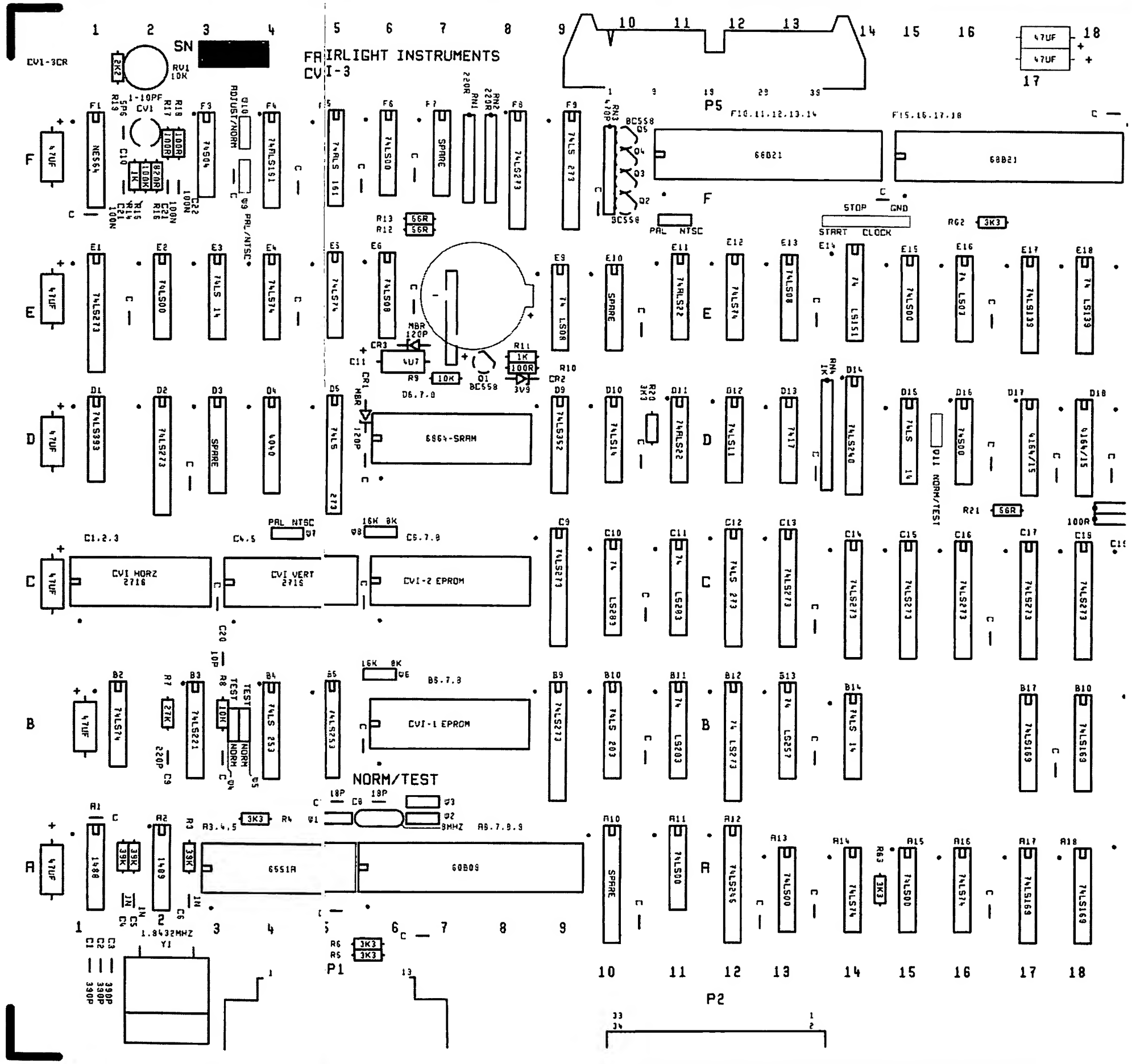
61. **Horizontal timing ROM** is 2Kx8 bits. It contains the data to generate eight horizontal control signals for one video line in both PAL and NTSC formats. The highest address bit of the ROM, which selects between PAL and NTSC timing data, is controlled by the vertical timing ROM. [C1 (CVI01 Sheet 8)]

62. **Horizontal timing decoder** combines the eight timing signals from the horizontal timing ROM to generate all the horizontal video and digital timing signals for the system, including the refresh timing and processor video access timing. [D2,E1,E4,E5 (CVI01 Sheet 8)]

63. **Vertical timing counter** addresses the vertical timing ROM sequentially. It is clocked by the line pulse from the horizontal timing ROM, and is cleared by the system vertical sync pulse from the sync selector (57). [D4 (CVI01 Sheet 8)]

64. **Vertical timing ROM** is 2Kx8 bits. It contains the data to generate eight vertical control signals for one video field in both PAL and NTSC formats. The highest address bit of the ROM selects between PAL and NTSC timing data. [C4 (CVI01 Sheet 8)

65. **Vertical timing decoder** combines the eight timing signals from the vertical timing ROM to generate all the vertical video and digital timing signals for the system, including processor interrupts. [D5 (CVI01 Sheet 8)]


FAIRLIGHT INSTRUMENTS
CVI-3
CVI-3CR
SN
RV1 10K
1-10PF CV1
P5
F10.11.12.13.14
F15.16.17.18
66D21
68B21
STOP
GND
START
CLOCK
PAL
NTSC
ADJUST/NORM
PAL/NTSC
6864-SRAM
D6.7.8
BC558
MBR 120P
R9 10K
R10 1K
100R
3V9
R13 56R
R12 56R
R21 56R
100R
R62 3K3
R63 3K3
R64 3K3
R5 3K3
R6 3K3
NORM/TEST
PAL NTSC
16K 8K
C1.2.3
C4.5
C5.7.8
B5.7.8
CVI HORZ 2716
CVI VERT 2715
CVI-2 EPROM
CVI-1 EPROM
6551A
6808
1.8432MHZ
Y1
P1
P2
Fairlight

PAL

Equipment Required
- Frequency meter, 100 MHz
- CVI-03 PAL aligned video board.
- Component overlay page 2.4.

Setup
- Remove the video board connector from P10.
- Set link W10 to ADJUST.
- Set link W7 to the position closest to link W8.
- Set link W9 to the position farthest from link W10.
- Set the link at board matrix F11 to the position closest to E10.
- Set RV1 to mid-range.
- Set RV2 fully clockwise.

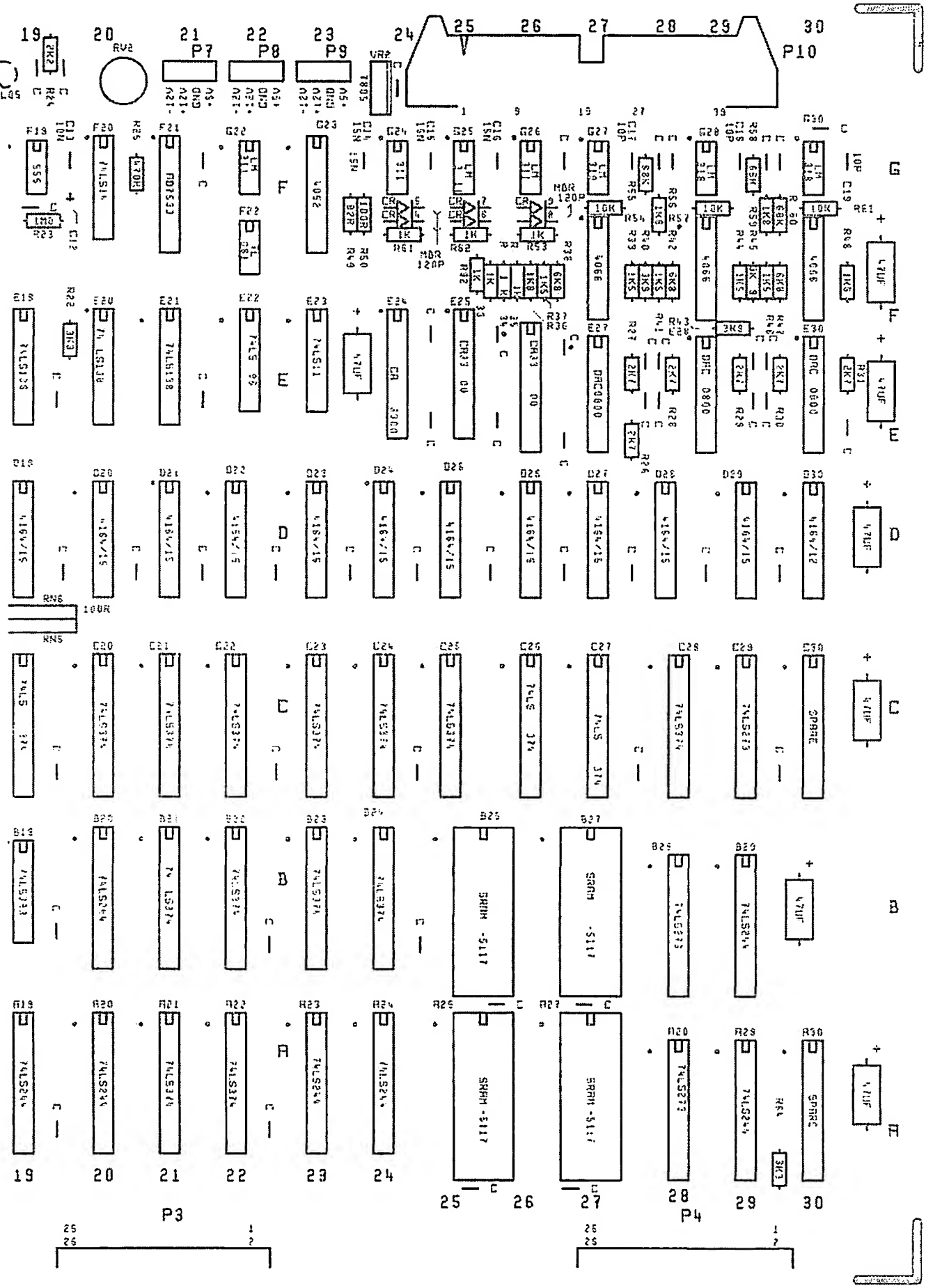
Procedure
- Measure the frequency at the NORM pin of W10.
- Adjust CV1 so that the frequency is 8.867MHz.
- Set link W10 to NORM.
- Reconnect the video board connector to P10.
- Measure the frequency at the NORM pin of W10. It should be 8.86723 MHz (+/- 10 Hz).

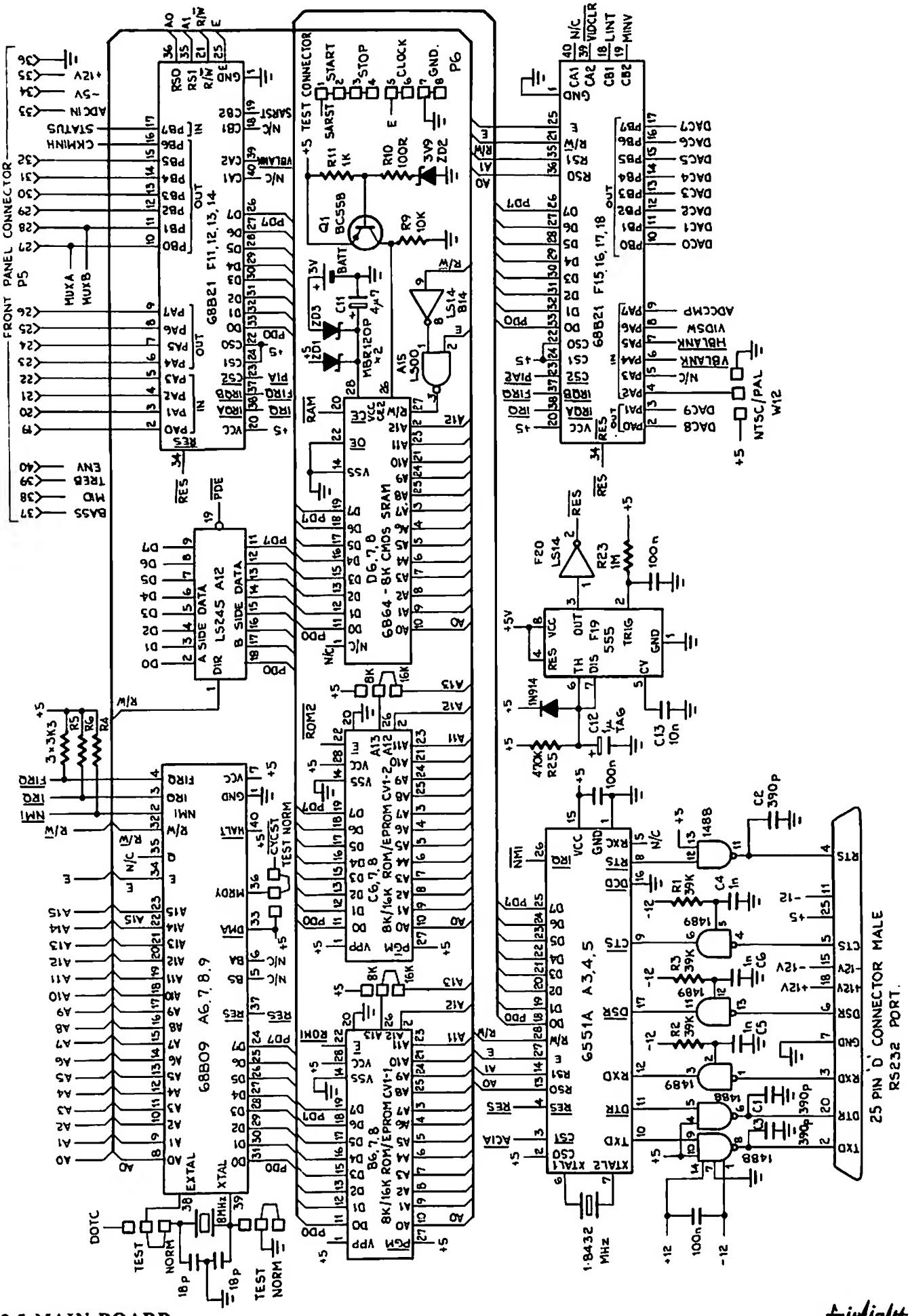
NTSC

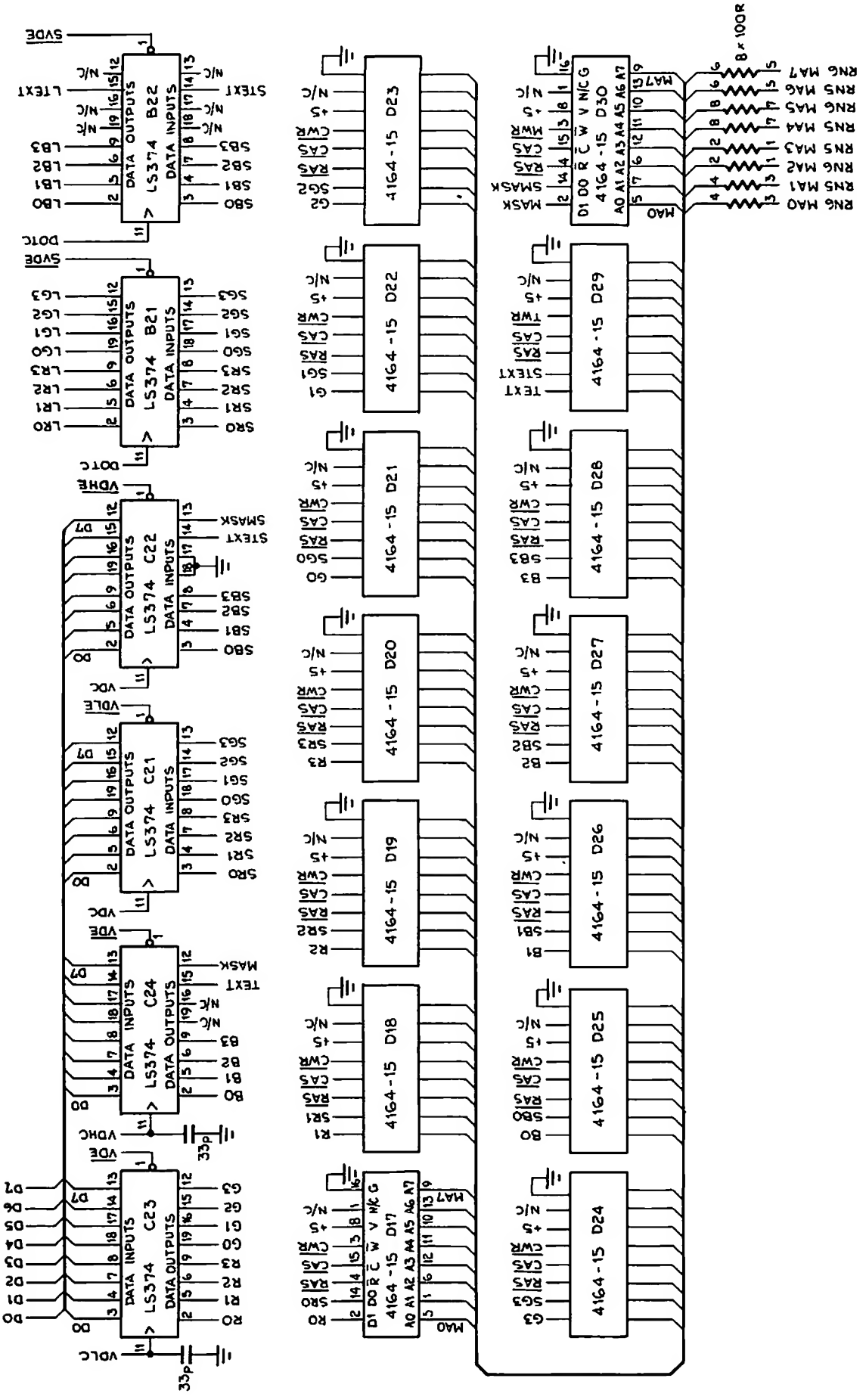
Equipment required
- Frequency meter, 100MHz.
- CVI-03 NTSC aligned video board.
- Component overlay page 2.4.

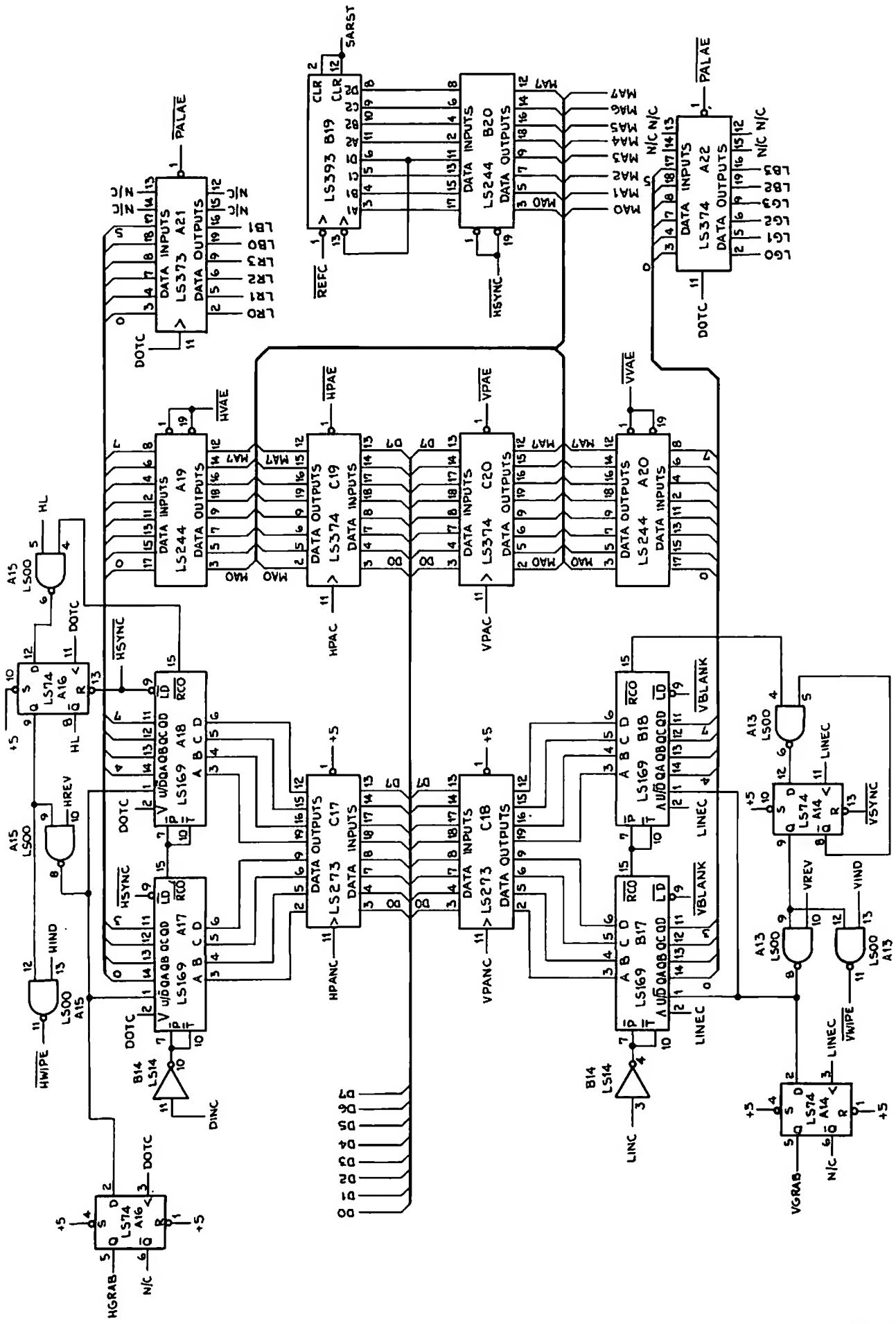
Setup
- Remove the video board connector from P10.
- Set link W10 to ADJUST.
- Set link W7 to the position farthest from link W8.
- Set link W9 to the position closest to link W10.
- Set the link at board matrix F11 to the position closest to E12.
- Set RV1 to mid-range.
- Set RV2 fully clockwise.

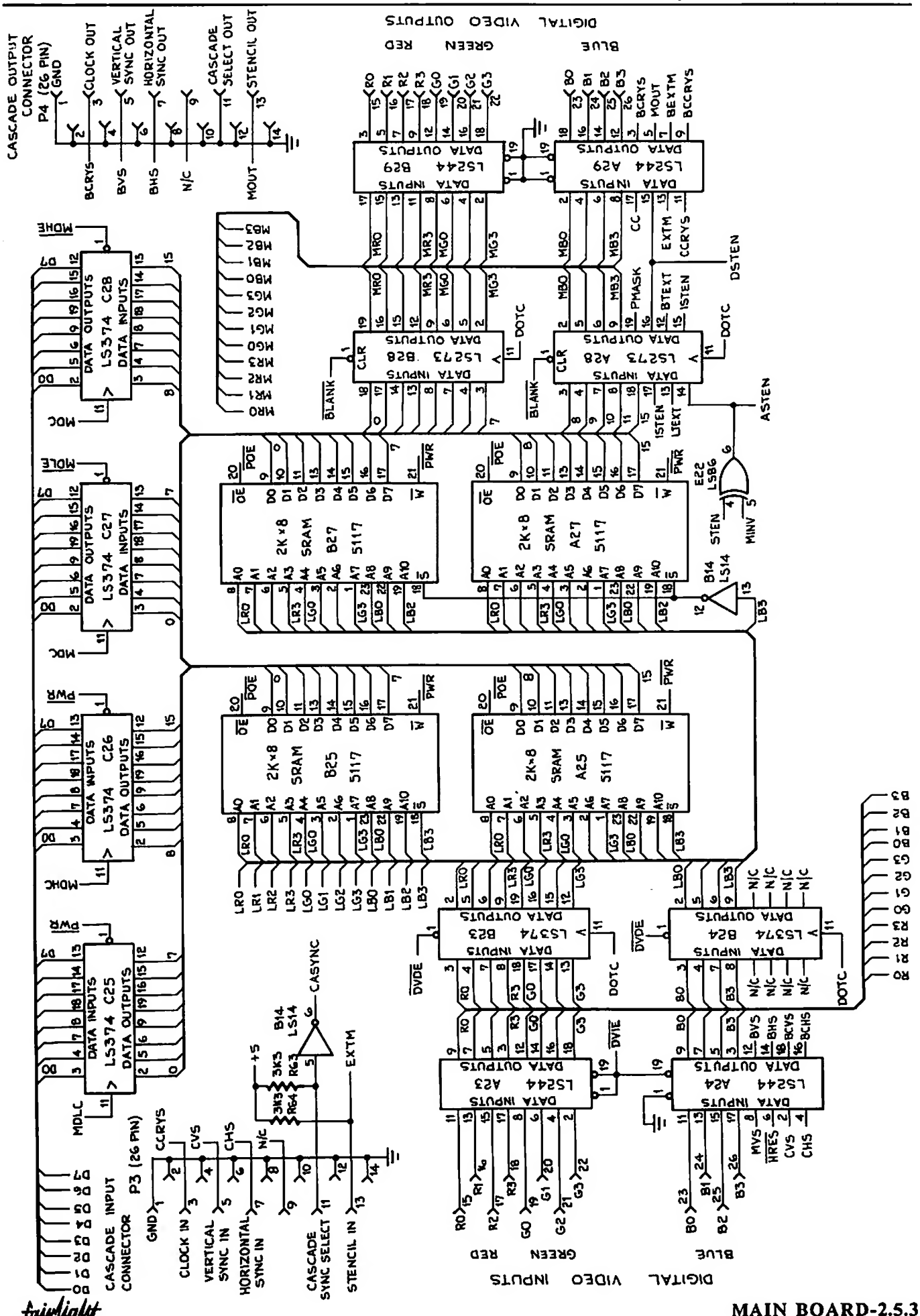
Procedure
- Measure the frequency at the NORM pin of W10.
- Adjust CV1 so that the frequency is 7.159MHz.
- Set link W10 to NORM.
- Reconnect the video board connector to P10.
- Measure the frequency at the NORM pin of W10. It should be 7.15909 MHz (+/- 10 Hz).

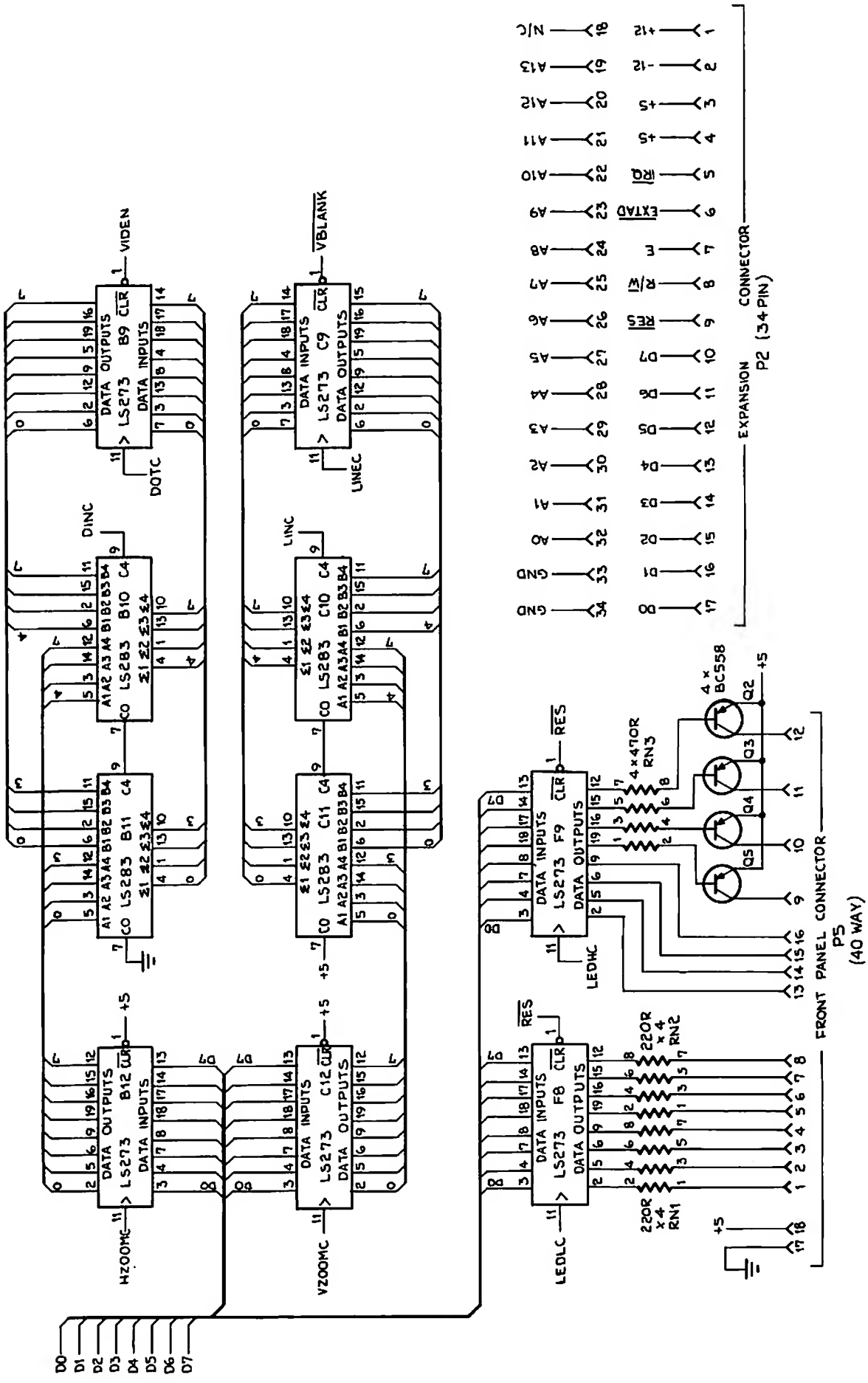

P3
P4
P7
P8
P9
P10
MAIN BOARD-2.4

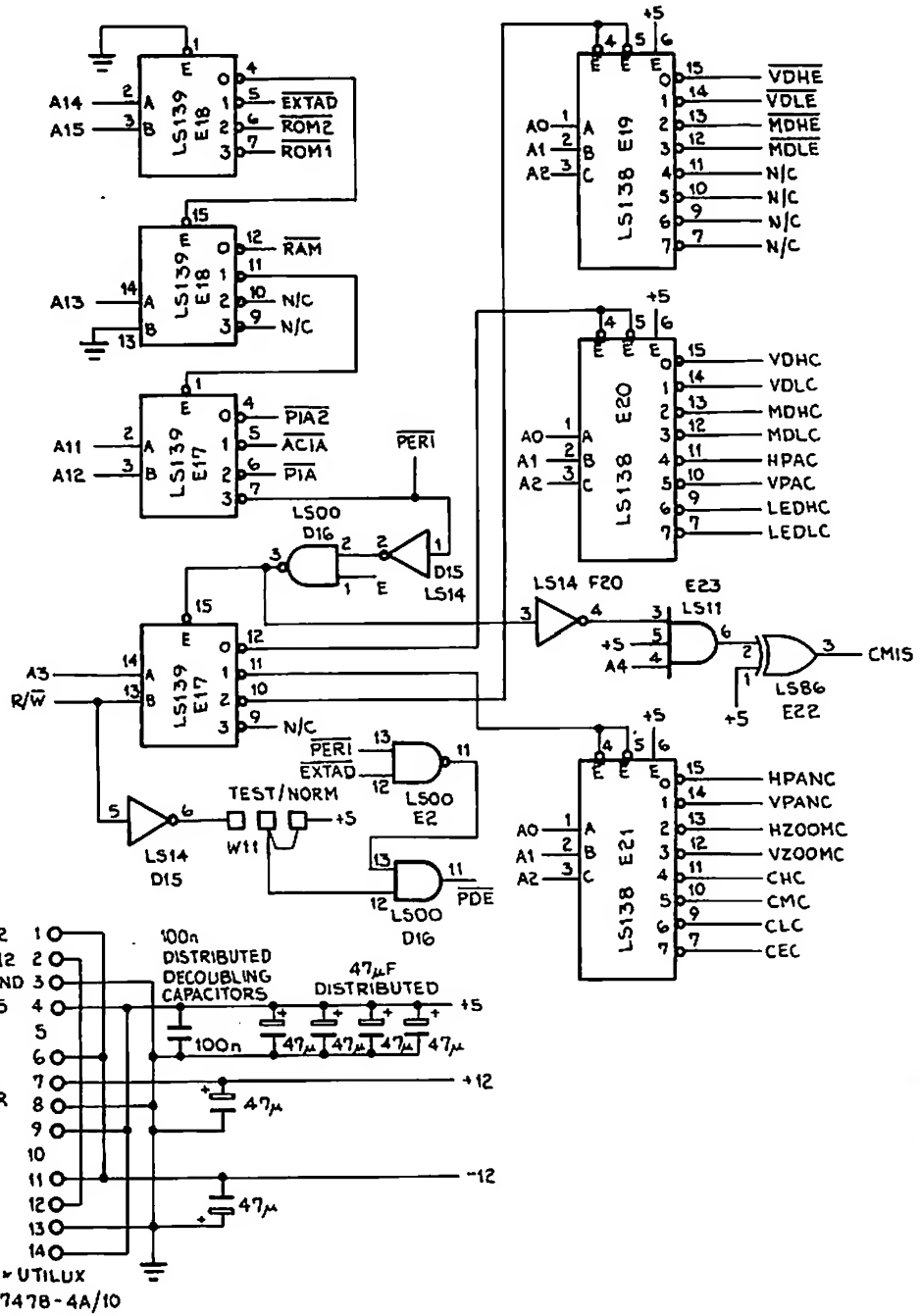

FRONT PANEL CONNECTOR
P5
+5 TEST CONNECTOR
P6
68B21 F11,12,13,14
68B21 F15,16,17,18
6B64 - 8K CMOS SRAM
D6,7,8
A12 A SIDE DATA B SIDE DATA
LS245
68B09 A6,7,8,9
6551A A3,4,5
C6,7,8 8K/16K ROM/EPROM CV1-2
B6,7,8 8K/16K ROM/EPROM CV1-1
555
LS14
1488
1489
1.8432 MHz
NTSC/PAL
25 PIN 'D' CONNECTOR MALE
RS232 PORT.


8 x 100R
RNG MA7
RNG MA6
RNG MA5
RNG MA4
RNG MA3
RNG MA2
RNG MA1
RNG MA0
MA7
MA0
4164-15 D30
4164-15 D29
4164-15 D28
4164-15 D27
4164-15 D26
4164-15 D25
4164-15 D24
4164-15 D23
4164-15 D22
4164-15 D21
4164-15 D20
4164-15 D19
4164-15 D18
4164-15 D17
LS374 B22
LS374 B21
LS374 C22
LS374 C21
LS374 C24
LS374 C23
33p
33p


LS393 B19
LS244 B20
LS374 A22
LS373 A21
LS244 A19
LS374 C19
LS374 C20
LS244 A20
LS374 A16
LS169 A18
LS273 C17
LS273 C18
LS169 B18
LS169 B17
LS169 A17
LS374 A14
LS374 A16
LS00 A15
LS00 A13
LS14 B14
SARST
REFC
HSYNC
PALAE
HVAE
HPAE
VPAE
VVAE
DOTC
HPAC
VPAC
HPANC
VPANC
HL
HREV
HIND
HWIPE
DINC
LINC
LINEC
VBLANK
VREV
VIND
VSYNC
VWIPE
VGRAB
HGRAB
N/C


CASCADE OUTPUT CONNECTOR P4 (26 PIN)
GND
CLOCK OUT
VERTICAL SYNC OUT
HORIZONTAL SYNC OUT
CASCADE SELECT OUT
STENCIL OUT
BCRYS
BVS
BHS
N/C
MOUT
DIGITAL VIDEO OUTPUTS
BLUE
GREEN
RED
LS244 A29
LS244 B29
LS273 A28
LS273 B28
LS374 C28
LS374 C27
LS374 C26
LS374 C25
2K x8 SRAM 5117
B27
A27
B25
A25
LS374 B24
LS374 B23
LS244 A24
LS244 A23
LS14 B14
LS86 E22
ASTEN
STEN
MINV
DSTEN
DOTC
BLANK
DVDE
DVIE
CASYNC
EXTM
MDHE
MDLE
MDHC
MDLC
PWR
CASCADE INPUT CONNECTOR P3 (26 PIN)
GND
CLOCK IN
VERTICAL SYNC IN
HORIZONTAL SYNC IN
CASCADE SYNC SELECT
STENCIL IN
CCRYS
CVS
CHS
N/C
DIGITAL VIDEO INPUTS
BLUE
GREEN
RED

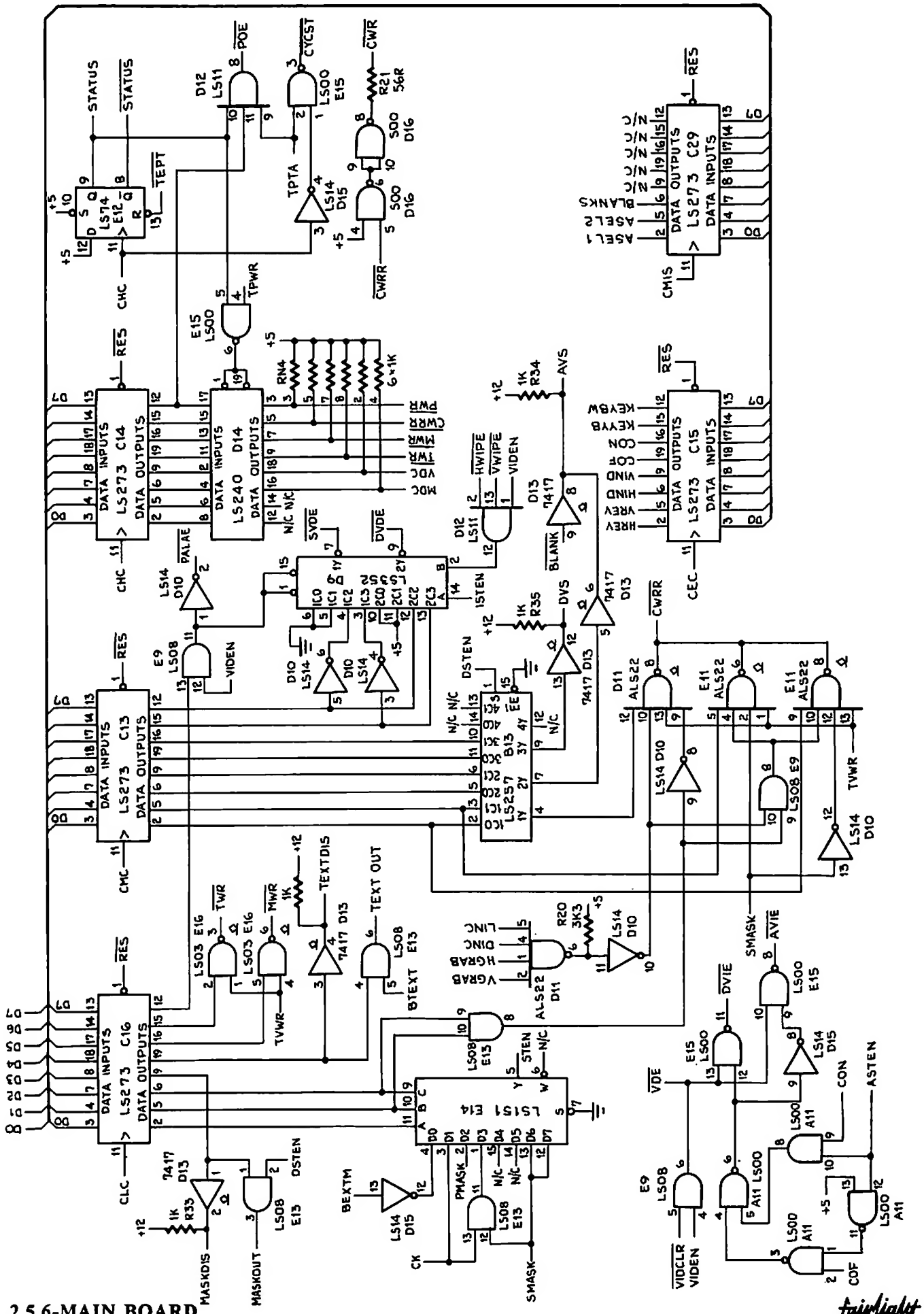

VIDEN
VBLANK
DOTC
LINEC
DINC
LINC
LS273 B9
LS273 C9
LS283 B10
LS283 B11
LS283 C10
LS283 C11
HZOOMC
VZOOMC
LS273 B12
LS273 C12
LS273 F8
LS273 F9
LEDLC
LEDHC
RES
+5
4 x BC558
Q2
Q3
Q4
Q5
4 x 470R RN3
220R x 4 RN1
220R x 4 RN2
FRONT PANEL CONNECTOR P5 (40 WAY)
EXPANSION CONNECTOR P2 (34 PIN)
D0
D1
D2
D3
D4
D5
D6
D7

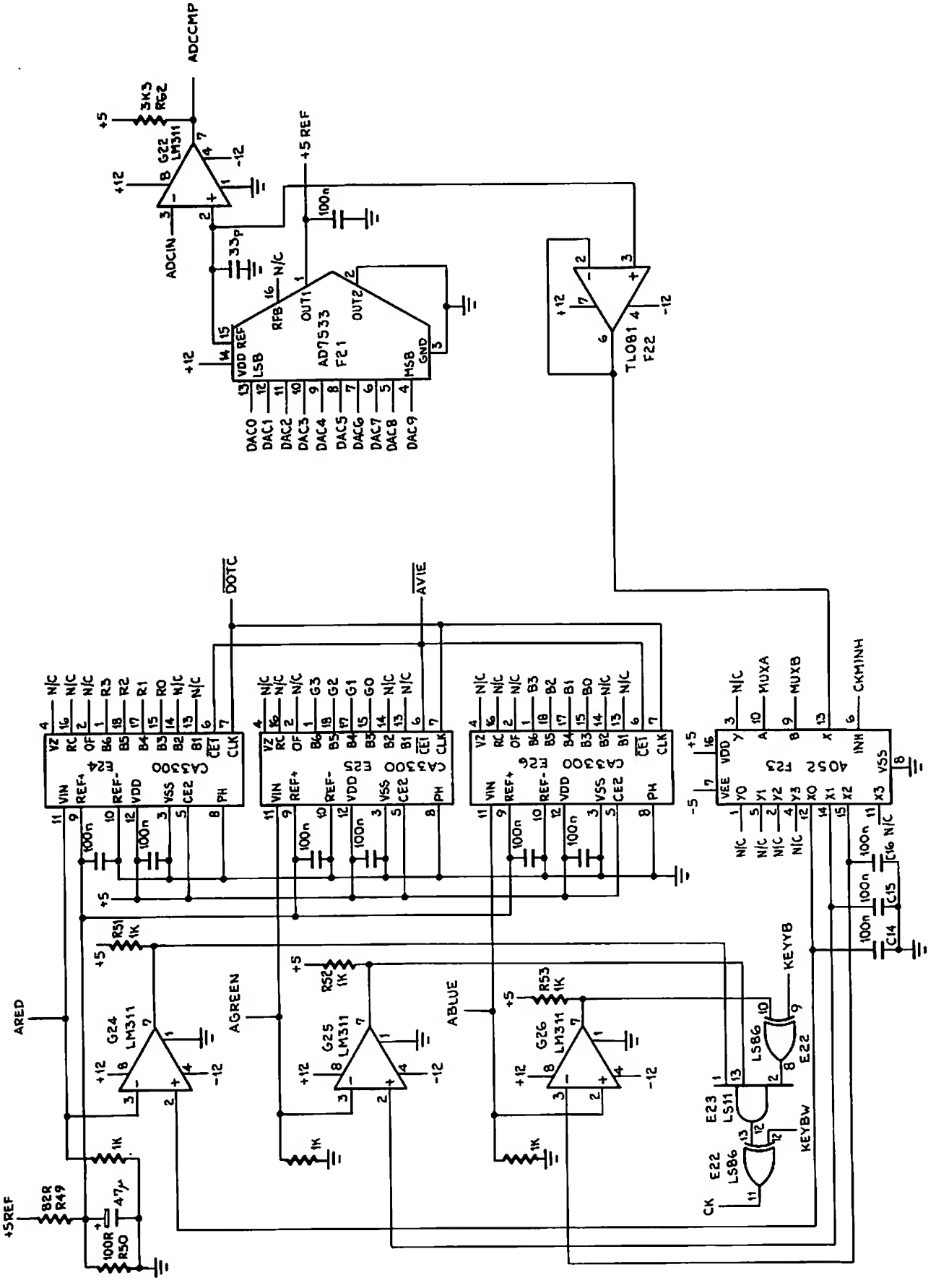


VIDEO I/O ADDRESS MAP

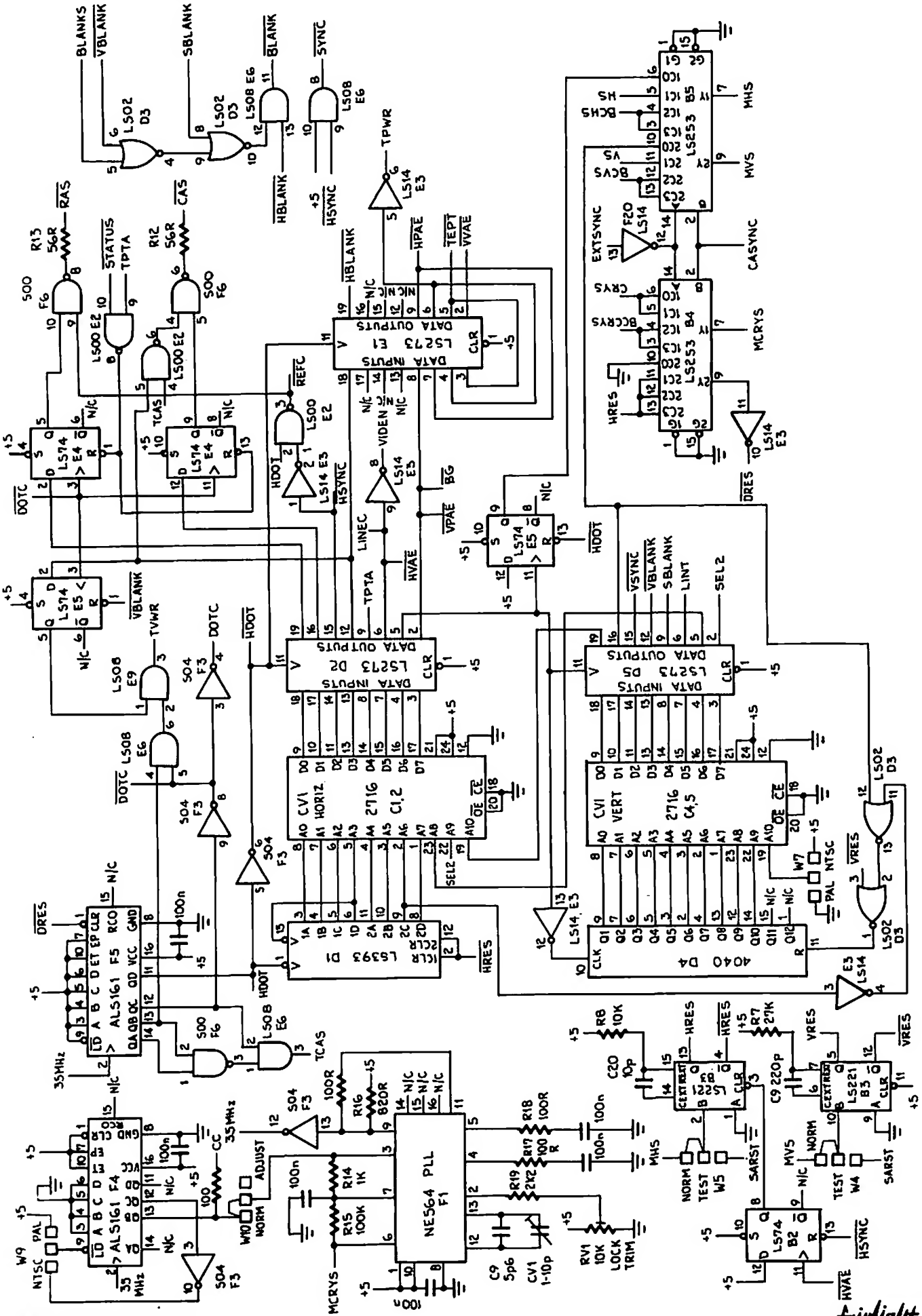
ADDRESS	WRITE FUNCTION	READ FUNCTION
3800	VRAM DATA HIGH	VRAM DATA HIGH
3801	VRAM DATA LOW	VRAM DATA LOW
3802	PALETTE DATA HIGH	PALETTE DATA HIGH
3803	PALETTE DATA LOW	PALETTE DATA LOW
3804	HORIZONTAL ADDRESS	—
3805	VERTICAL ADDRESS	—
3806	LEDS HIGH	—
3807	LED LOW	—
3808	HORIZONTAL PAN	—
3809	VERTICAL PAN	—
380A	HORIZONTAL ZOOM	—
380B	VERTICAL ZOOM	—
380C	CONTROL HIGH	—
380D	CONTROL MID	—
380E	CONTROL LOW	—
380F	CONTROL EFFECTS	—
3810	CONTROL MISC.	—

ADDRESS MAP		I/O ADDRESS MAP	
0000 - 1FFF	RAM	2000 - 27FF	PIA2
2000 - 3FFF	I/O	2800 - 2FFF	ACIA
4000 - 7FFF	EXTERNAL	3000 - 37FF	PIA1
8000 - BFFF	ROM 2	3800 - 3FFF	VIDEO I/O
C000 - FFFF	ROM 1		

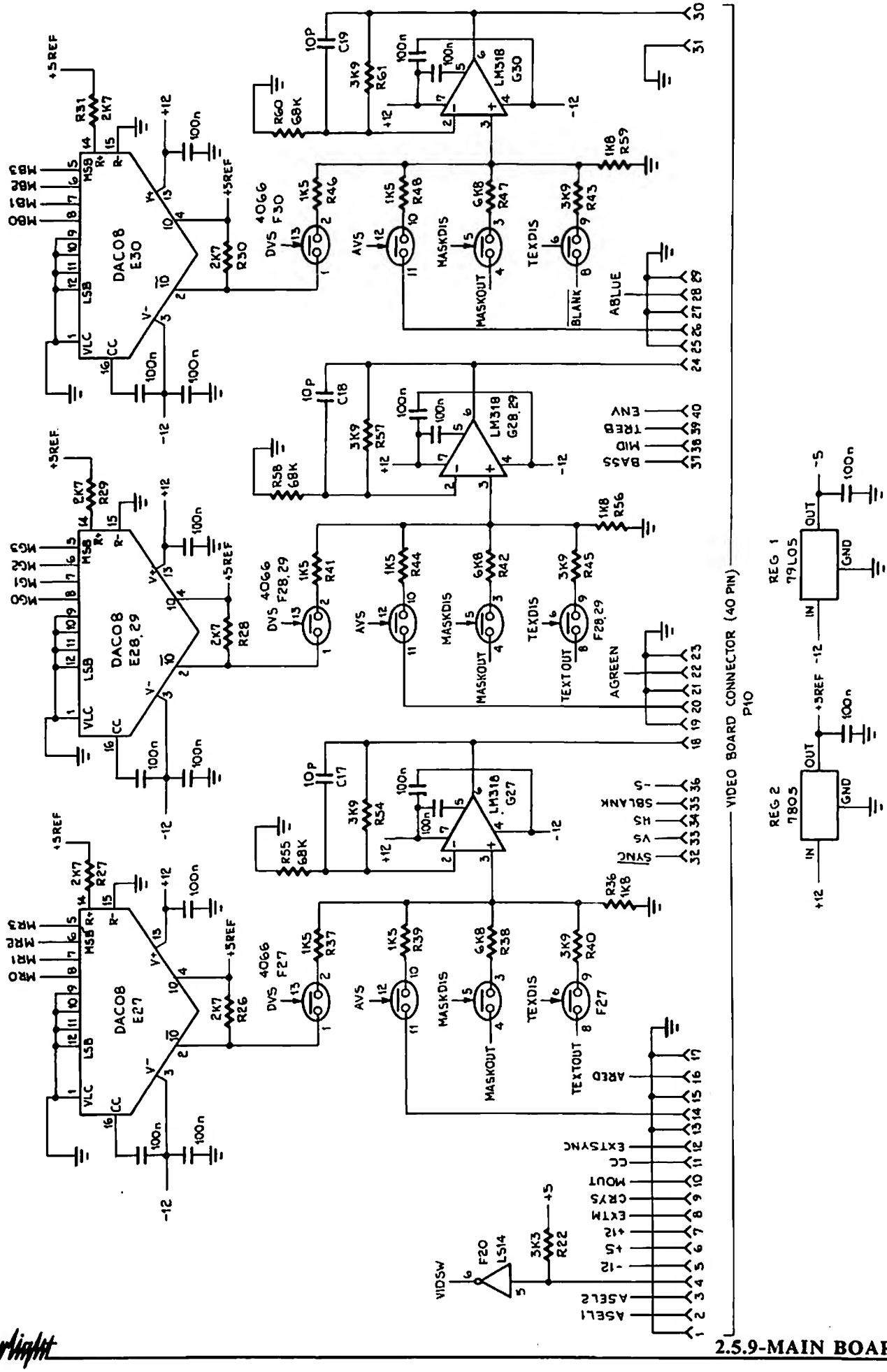

STATUS
STATUS
TEPT
CHC
RES
POE
CYCST
CWR
TPTA
TPWR
CWRR
SVDE
DVDE
PALAE
ISTEN
VIDEN
HWIPE
VWIPE
BLANK
HREV
VREV
HIND
VIND
COF
CON
KEYB
KEYBW
CEC
CMIS
DSTEN
TWR
MWR
TEXTDIS
TEXT OUT
BTEXT
LINC
DINC
HGRAB
VGRAB
SMASK
AVIE
DVIE
VDE
CON
ASTEN
VIDCLR
COF
MASKDIS
MASKOUT
BEXTM
CK
PMASK_2
STEN
DSTEN
AVS
DVS
TVWR
CLC
CMC
CHC
DATA INPUTS
DATA OUTPUTS
LS273 C14
LS240 D14
LS273 C15
LS273 C29
LS273 C13
LS273 C16
LS257 B13
LS151 E14
LS74 E12
LS14 D10
LS14 D15
LS00 E15
LS00 D16
LS11 D12
LS08 E9
LS08 E13
LS03 E16
LS22 D11
LS00 A11
7417 D13
RN4
R21 56R
R34 1K
R35 1K
R33 1K
R20 3K3

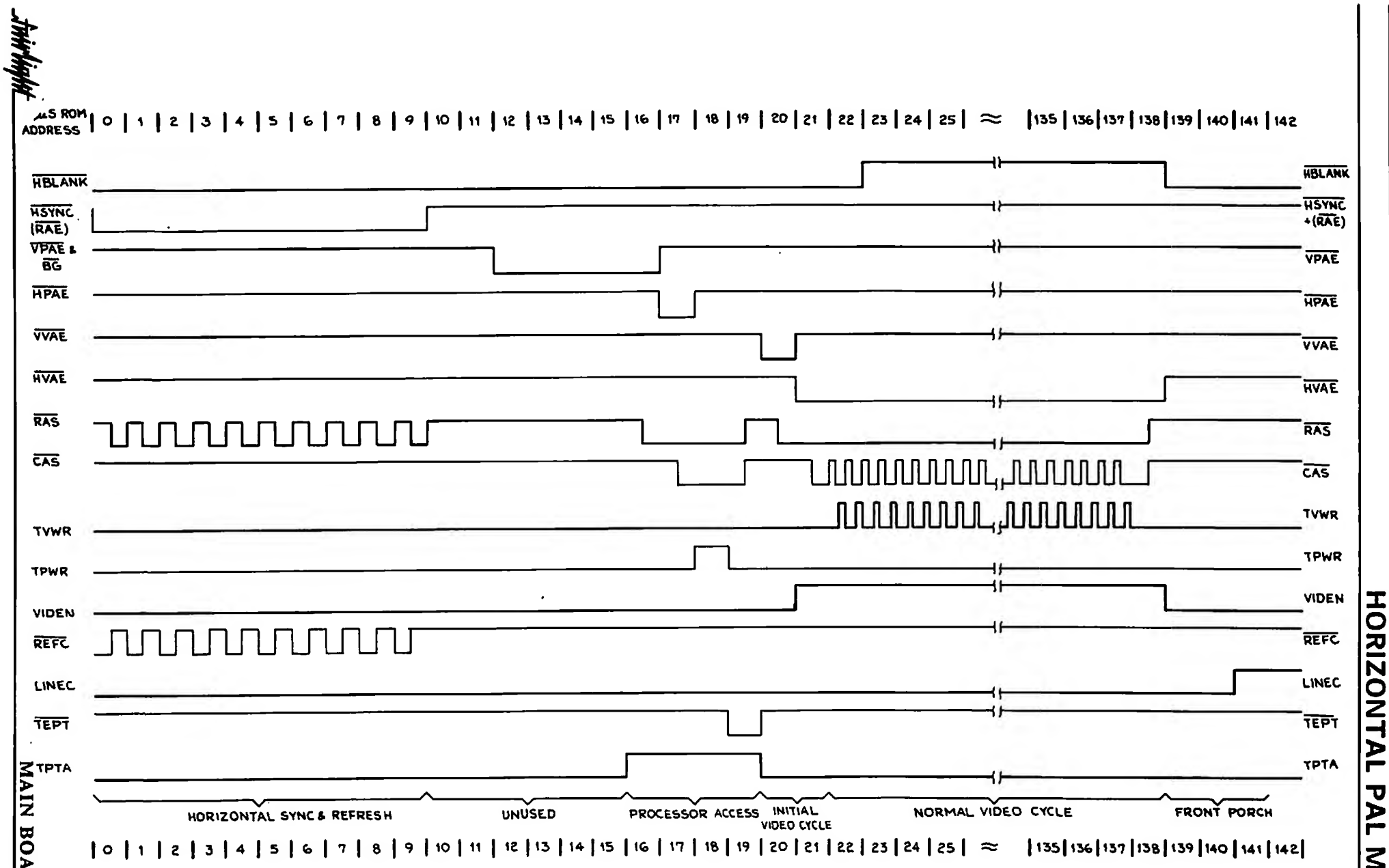

ADCCMP
ADCIN
+5 REF
AD7533
TL081
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
DAC8
DAC9
DOTC
AVIE
CKMINH
MUXA
MUXB
ARED
AGREEN
ABLUE
KEYB
KEYBW
+5REF
LM311
LS86
LS11

TIMING GENERATION AND SYNC



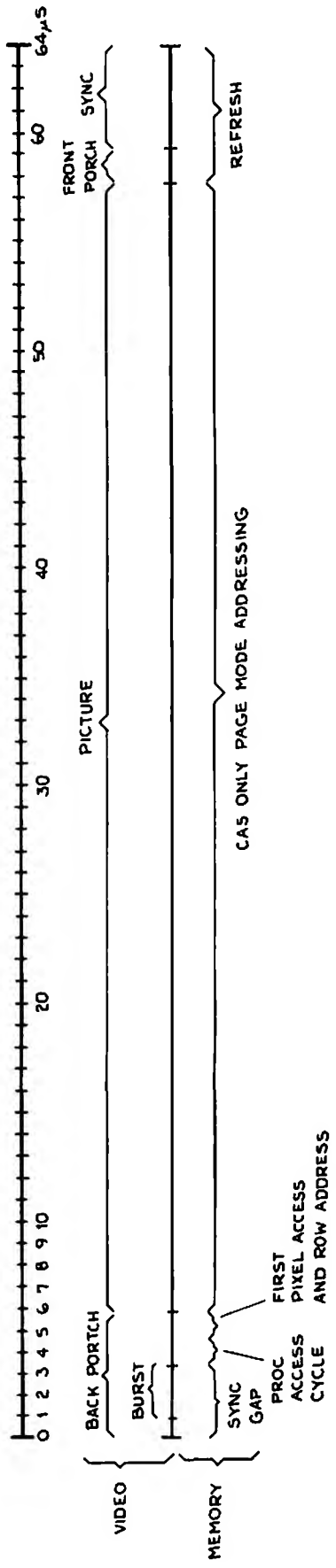
fairlight


DAC08 E30
DAC08 E28,29
DAC08 E27
4066 F30
4066 F28,29
4066 F27
LM318 G30
LM318 G28,29
LM318 G27
LS14 F20
REG 1 79L05
REG 2 78L05
VIDEO BOARD CONNECTOR (40 PIN) P10
ABLUE
AGREEN
ARED
ENV
TREB
MID
BASS
SYNC
SBLANK
-5
HS
VS
EXTSYNC
CC
MOUT
CRYS
EXTM
+12
+5
-12
ASEL2
ASEL1
VIDSW

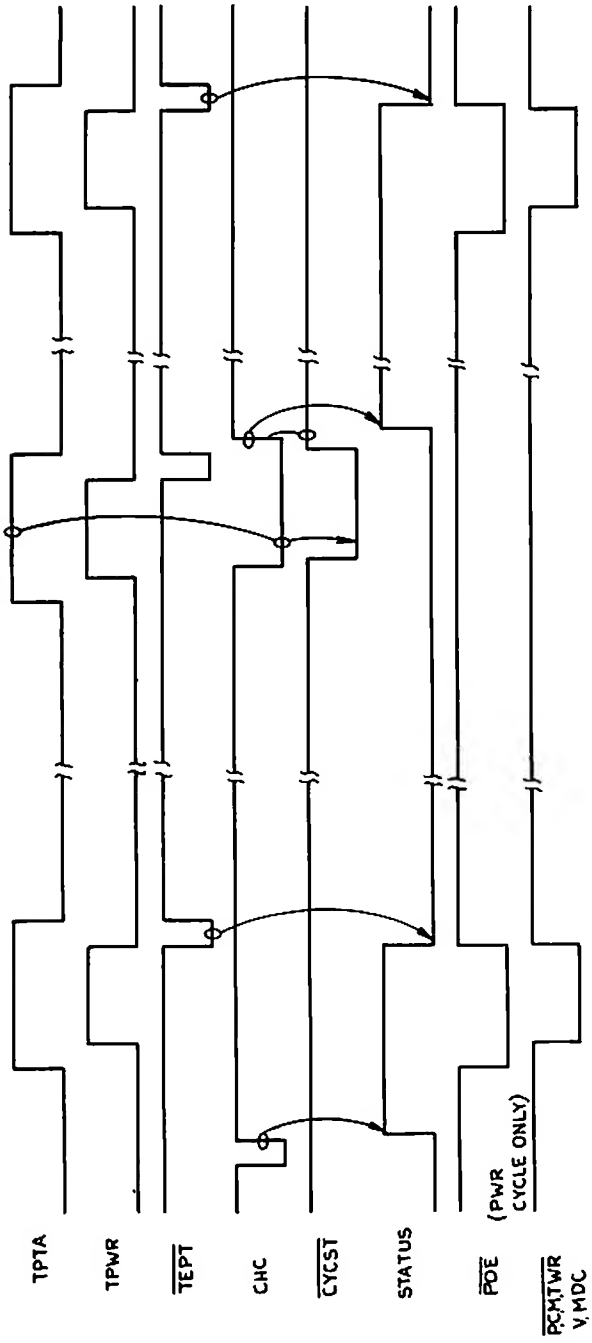


HORIZONTAL PAL MODE

PAL TIMING



PARAMETER	PAL	NTSC	UNITS
No OF CC CYCLES/LINE	283·7516	227·301	
FRAME FREQUENCY	25	30	Hz
LINE FREQUENCY	15625	15750	Hz
LINE PERIOD	64	63·492	µS
No LINES/FRAME	625	525	MHz
COLOUR CARRIER	4·7		µS
BLANKING	12·05		µS
FRONT PORCH	1·55		µS
BACK PORCH	5·8		µS
BURST DURATION	5·25		µS
BURST START	5·6		µS
ACTIVE VIDEO	51·95		µS
BURST AMPLITUDE	300		mV
SIGNAL VOLTAGE	700		mV
SYNC VOLTAGE	300		mV



VRAM READ SEQUENCER

1	[CHECK STATUS=LOW]
2	WRITE PIXEL ADDRESS
3	WRITE CONTROL LATCH HIGH WITH
	00001000_2
4	WAIT FOR STATUS=LOW
5	READ DATA FROM VRAM READ (H,L)

VRAM WRITE SEQUENCE

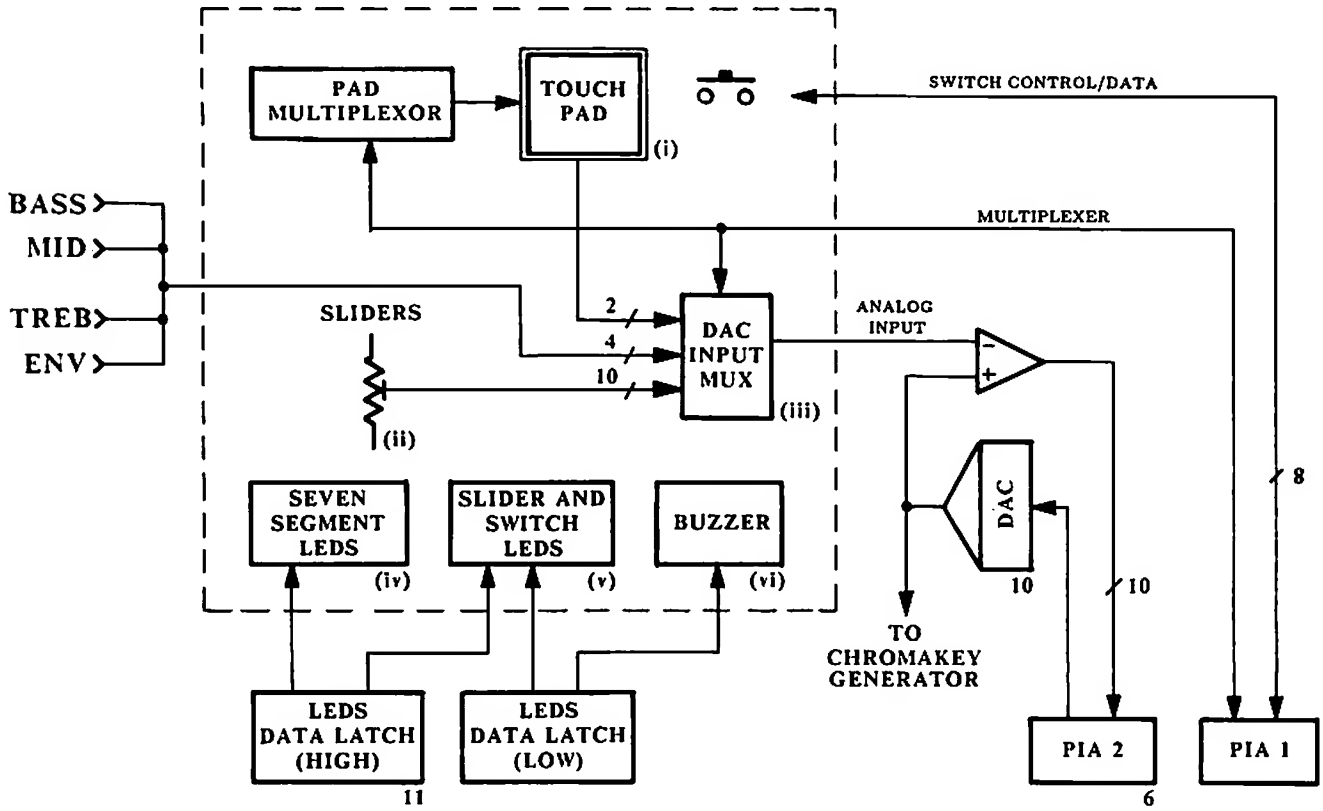
1	[CHECK STATUS = LOW]
2	WRITE PIXEL ADDRESS
3	WRITE DATA TO VRAM WRITE (H,L)
4	WRITE CONTROL LATCH HIGH WITH
	$0\,CMT\,000_2$
	WHERE C = COLOUR
	M = MASK WRITE
	T = TEXT WRITE

PALETTE READ SEQUENCE

1	[CHECK STATUS = LOW]
2	WRITE COLOUR TO BE READ TO
	VRAM WRITE (H,L)
3	WRITE CONTROL LATCH HIGH WITH
	00000100_2
4	WAIT FOR STATUS=LOW
5	READ PALETTE DATA FROM
	MAP READ (H,L)

PALETTE WRITE SEQUENCE

1	[CHECK STATUS = LOW]
2	WRITE COLOUR TO BE CHANGED
	TO VRAM WRITE (H,L)
3	WRITE PALETTE DATA TO MAP
	WRITE (H,L)
4	WRITE CONTROL LATCH HIGH WITH
	10000000_2
	[ONLY NECESSARY <64μS AFTER WRITE



1. **Touch-sensitive pad**, under the control of two multiplexers, produces four voltages which are decoded to determine the pad touch position. The multiplexers are controlled from PIA1. [U3,U4]

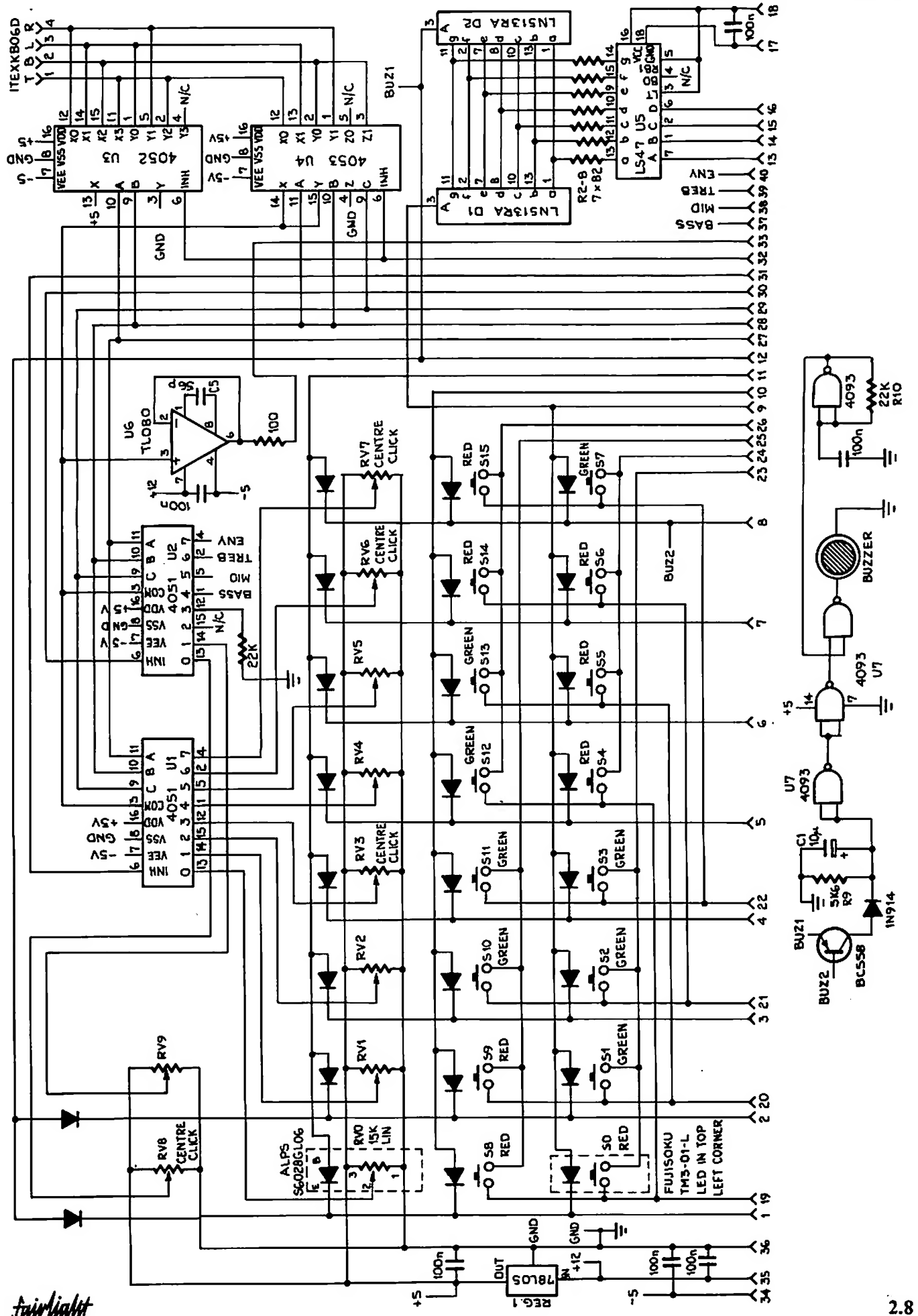
2. **Front panel pots** each generate a voltage according to the slider position, which may be digitised by the ADC under software control.

3. **Seven-segment leds** are controlled by a seven-segment decoder/driver using four bits from the LEDs control latch. [U5,D1,D2]

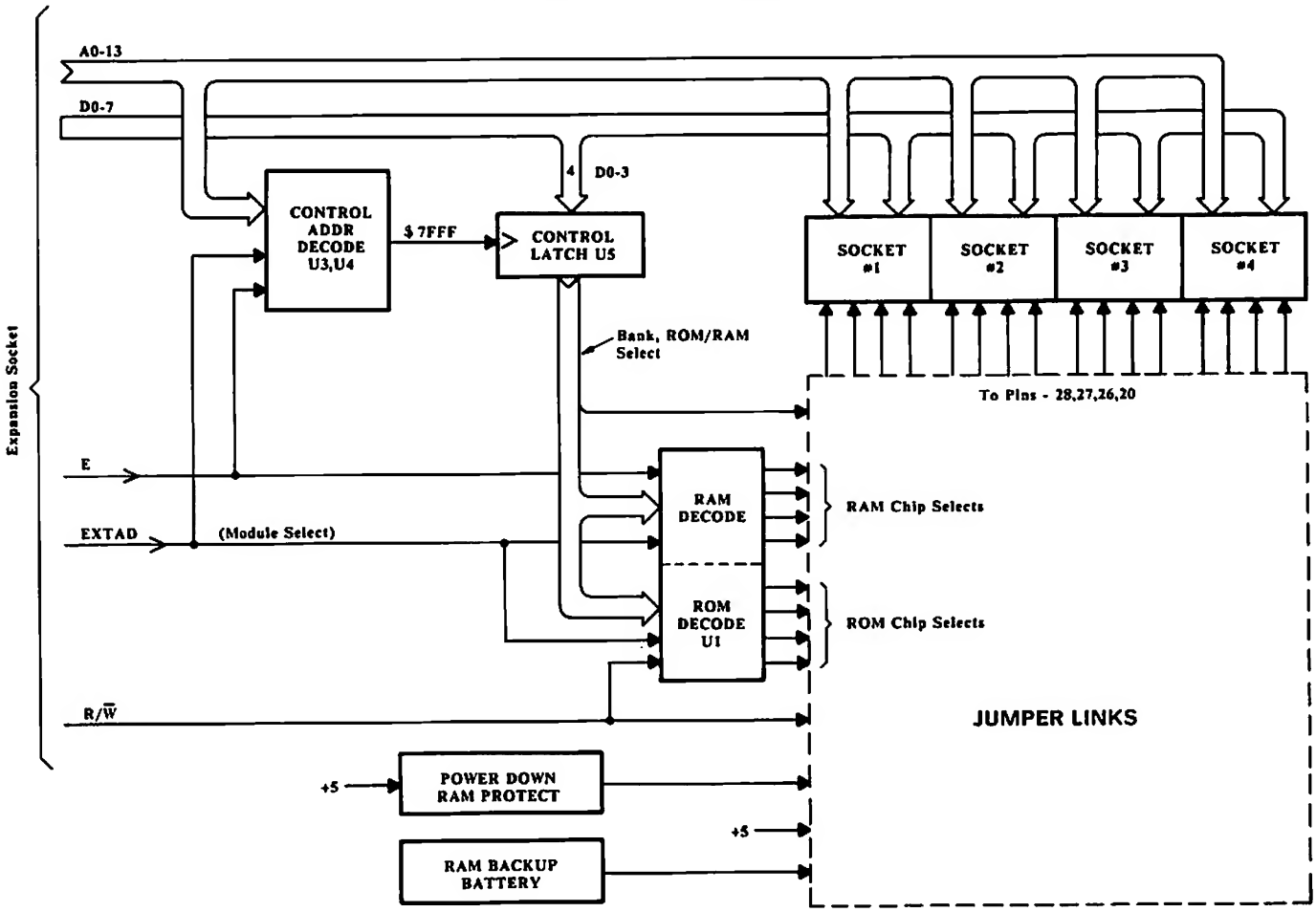
4. **Front-panel leds** on the pots and switches are arranged in a 4x8 multiplexing matrix controlled by 12 bits from the LEDs control latch. Each LED is updated 50-60 times per second.

5. **Buzzer** oscillator is enabled using a position in the front-panel multiplexing matrix (4). [U7]

6. **Analog-input multiplexer** selects the input to the analog-to-digital converter from the front-panel slider voltages, the touch-pad voltages and the audio-analyser levels (bass, mid-range, treble and envelope). The multiplexer is controlled from PIA1. [U1,U2,U6]


ITEXKB06D
4052 U3
4053 U4
LN513RA D2
LN513RA D1
R2-8 7×82
LS47 U5
BUZ1
BUZ2
BUZ21
BUZ22
BUZZER
U6 TL080
100
22K
RV1
RV2
RV3 CENTRE CLICK
RV4
RV5
RV6 CENTRE CLICK
RV7 CENTRE CLICK
RV8 CENTRE CLICK
RV9
RV0 15K LIN
ALPS SG028GL06
FUJISOKU TM3-01-L LED IN TOP LEFT CORNER
4051 U1
4051 U2
4093 U7
1N914
BC558
5K6 R9
22K R10
100n
10µ C1
78L05 REG 1
GND
+5
-5
+12
-5V
BASS
MID
TREB
ENV
RED
GREEN

BLOCK DIAGRAM



General

The memory expansion module plugs into the "expansion bus" socket on the back of the CVI. It allows up to 128K bytes of EPROM or 64K bytes of static battery RAM (or various mixes of EPROM and RAM) to be added to the CVI system memory. The memory on the module exists as a number of 16K byte banks which are selected under software control to appear in the 16K expansion bus address space, at 4000 to 7FFF.

Functional description

1) Control address decode. The 16 input AND gate formed of U3 and U4 decodes the top address within the 16K byte expansion module address space. This is used to select the mode control register.

2) The mode control register. U5, is a 4 bit, write only latch. By writing to this register, the processor selects which of the "socket(s)" appears in the 16K byte address space, and whether they are ROM or RAM.

Table 1. The functions of the control register are:

B1	B0	JUMPER 8K/16K RAM	SOCKETS SELECTED	
0	x	8K	#1 - Lower 8K RAM, #2 - Upper 8K RAM	
1	x		#3 - Lower 8K RAM, #4 - Upper 8K RAM	
0	0	16K	#1	ROM or RAM
0	1		#2	
1	0		#3	
1	1		#4	

B2 - Only used by 32K byte ROMS, for which it is used as A14, selecting the upper or lower half of the ROM.

B3 - A1 selects the RAM decoder, A0 selects the ROM decoder.

Table 2

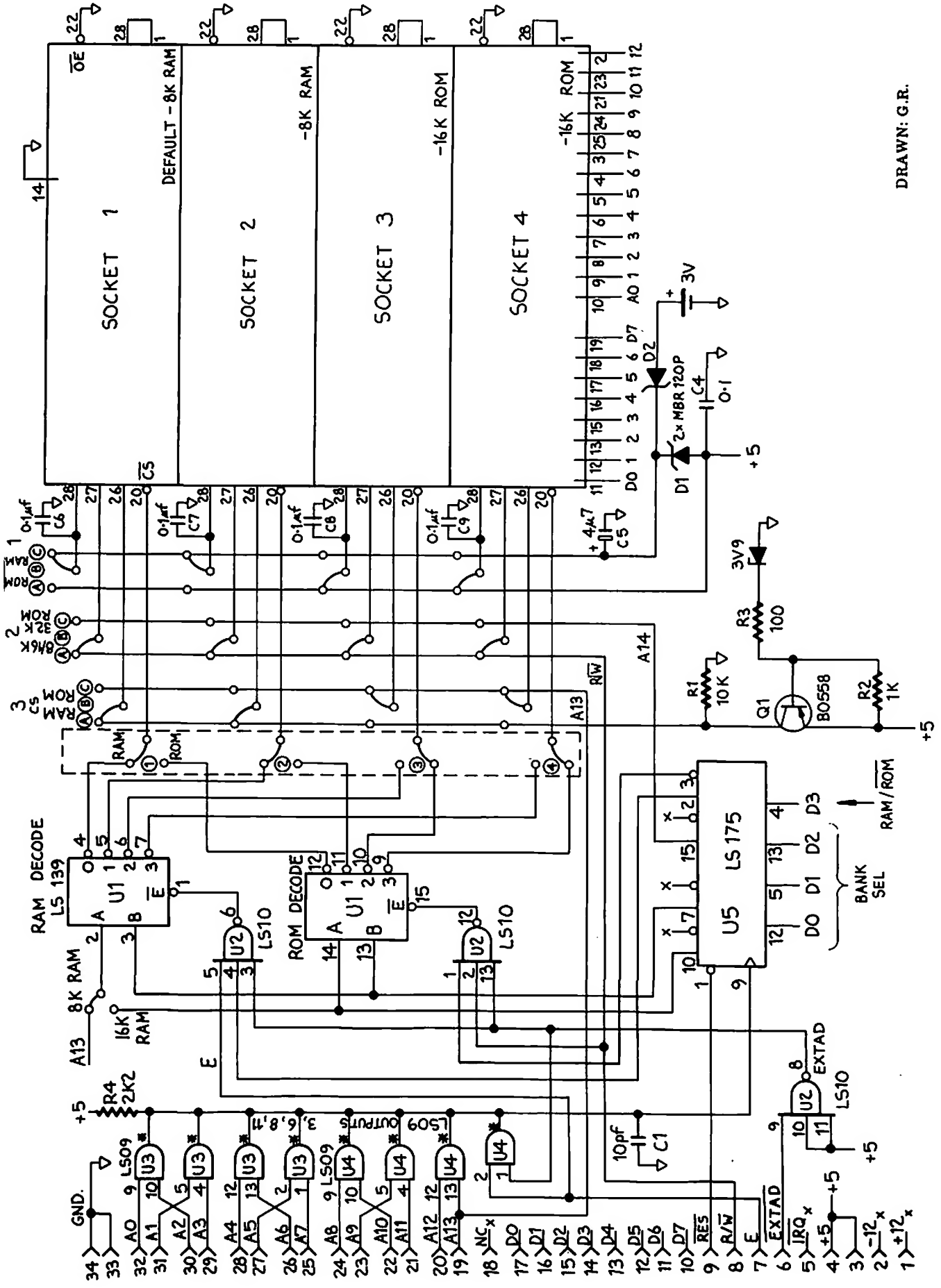
SOCKET PIN#	6264 8K BYTE RAM	27128 16K BYTE ROM	27256 32K BYTE ROM
28	Vcc (Battery backed)	Vcc (+5)	Vcc (+5)
27	$\overline{WE}$ (R/W)	$\overline{PGM}$ (R/W or A14 = 1)	A14
26	$\overline{CS}$ (Disable)	A13	A13
20	$\overline{CS}$ (RAM Decoder)	$\overline{CE}$ (ROM Decoder)	$\overline{CE}$ (ROM Decoder)

3) Power down RAM protect. Q1 and the 3.9V zener provide a DISABLE signal for any RAM IC's on the module, which are also supported by a 3V lithium battery.

4) The RAM/ROM decoder U1 provides the four RAM select and four ROM select signals which are connected by jumper links to the appropriate sockets.

5) Memory sockets. The four 28 pin IC sockets are each individually configurable to hold 8K byte RAMS, 16K ROMS or 32K ROMS. Normally, the devices used and the connections on the 4 jumper selectable pins are as per Table 2 above.

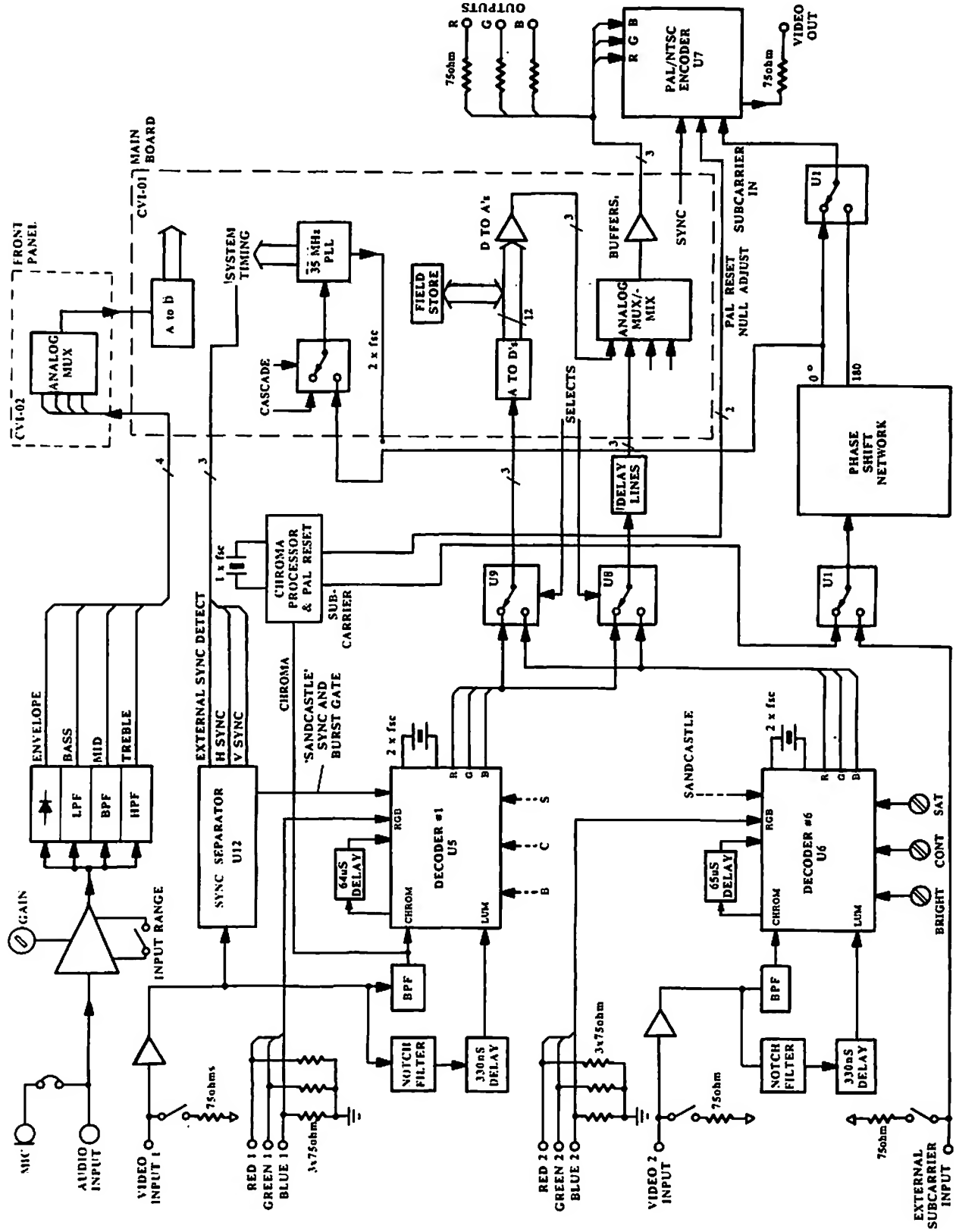
6) The Jumper Links. Each socket has 4 "double throw" links, i.e the centre pad must be linked to one of the two pads to either side of it. Refer to the circuit diagram for their names and functions.


SOCKET 1
SOCKET 2
SOCKET 3
SOCKET 4
DEFAULT - 8K RAM
-8K RAM
-16K ROM
-16K ROM
DRAWN: G.R.
RAM DECODE LS 139
ROM DECODE
LS10
LS175
BANK SEL
RAM/ROM
8K RAM
16K RAM
LS09 OUTPUTS
EXTAD
3V
3V9
+5
GND.
R1 10K
R2 1K
R3 100
R4 2K2
Q1 BC558
10pf C1
2x MBR 120P
0·1µf
4µ7

Video Board - PAL 3

CONTENTS

CVI-07 Chroma board


OUTPUTS
R
G
B
75ohm
PAL/NTSC ENCODER U7
R G B
VIDEO OUT
MAIN BOARD
CVT-01
FRONT PANEL
CVT-02
ANALOG MUX
A to b
SYSTEM TIMING
35 MHz PLL
CASCADE
2 x fsc
FIELD STORE
D TO A's
A TO D's
12
BUFFERS.
SYNC
ANALOG MUX/-MIX
SUBCARRIER IN
PAL RESET NULL ADJUST
SELECTS
DELAY LINES
PHASE SHIFT NETWORK
0°
180
U1
U9
U8
CHROMA PROCESSOR & PAL RESET
1 x fsc
SUB-CARRIER
CHROMA
'SANDCASTLE' SYNC AND BURST GATE
EXTERNAL SYNC DETECT
H SYNC
V SYNC
ENVELOPE
BASS
MID
TREBLE
LPF
BPF
HPF
SYNC SEPARATOR U12
2 x fsc
DECODER #1 U5
RGB
CHROM
LUM
64uS DELAY
BPF
NOTCH FILTER
330nS DELAY
SANDCASTLE
DECODER #6 U6
65uS DELAY
SAT
CONT
BRIGHT
GAIN
INPUT RANGE
MIC
AUDIO INPUT
VIDEO INPUT 1
75ohms
RED 1
GREEN 1
BLUE 1
3x75ohm
RED 2
GREEN 2
BLUE 2
VIDEO 2 INPUT
EXTERNAL SUBCARRIER INPUT

Audio input

The audio input is selected from either the internal microphone or an external source. The external source is selected when a plug is inserted into the audio input jack on the back panel. [CVI03-1]

Audio amplifier

The audio amplifier amplifies the selected input signal to levels required by the following filter and detector stages. The gain of the amplifier may be set to low or high using Switch 1 No.1 (SW1/1), and adjusted using the Audio Sensitivity control. [U2,U4, CVI03-5]

Audio analyser

The audio analyser consists of three filters: lowpass (200Hz) for bass, bandpass (400-800Hz) for midrange, highpass (800Hz) for treble. The output of each filter drives an envelope detector, the output voltages of which represent the energy in that particular audio bandwidth. A fourth detector is used to detect the overall envelope. These four signals (0-3.2V) are passed to the analog multiplexer on the front panel and on to the ADC. [U4, CVI03-5]

Sync separator

U12 and associated circuitry derives various video timing signals from the video signal on the Video 1 input. When U12 determines that the external video is absent or poor quality then pin U12/9 sources current into its load resistor R163, causing the output of U11/7 to go high. With acceptable external video present U12/9 goes open circuit, resulting in a low output from U11/7. This signal is used on the main board to select the appropriate internal or external timing signals. When acceptable external video is present U12/1 otputs positive going vertical sync pulses which are buffered by U13/3,4. When no external video is present these pulses are inhibited. U12/15 produces a positive going, multilevel synchronising pulse that is used by the decoders. The lower level provides Hsync timing and the higher level provides burst gating. Comparator U10 detects H.sync from the sandcastle for the main board timing. A vertical blanking signal (SBLANK) from the main board is added to the sandcastle signal by R150 and CR5. The resultant signal is used by the decoders U5 and U6. IC U15 buffers the signal to the decoders.

Internally the 3571 consists of a sync separator, oscillator, phase-locked loop, a vertical sync integrator and a 625 line divider. The sync separator samples the input video black level on U12/4, R162, C113 and generates a sync slicing level proportional to the input sync amplitude via R161, U12/3. The oscillator runs at 2H frequency which is set by C108, R154, RV10 and the voltage on pin 17 and is phase locked to the external video H via the RC networks on U12/7,17,11 and 6. The response time of the phase lock loop is made slow or fast depending on whether the oscillator is locked or not by clamping or open circuiting U12/11. The vertical sync integrator and detector is formed by U12/5, R159 and C112. The 625 line divider, coincidence detection and signal switch is used to generate the vertical sync output in two different ways depending on the quality of the external video. The Vsync can be generated internally by the divider or taken from the external sync integrator.

Video input buffers

These consist of emitter followers Q9 and Q11 buffer the video 1 and 2 inputs. Their outputs drive the bandpass and notch filters for the two decoder ICs. Q9 (input 1) also provides the video signal to the sync separator U12. [CVI03-2 and 3]

Notch filters

These are formed by L4, C40 and L9, C68 removes the colour subcarrier (4.4MHz in PAL) from the composite video signal. The remaining luminance information at the output is passed to the decoders via the 330nS delay lines. [CVI03-2 and 3]

Bandpass filters

These are formed by L3, C37 and L8, C65 passes only the colour subcarrier component of the incoming video signal to the chrominance input of decoders. Chroma from VIDEO 1 is also used by the chroma processor. [CVI03-2 and 3]

330nS Delay line

This delay line in the luminance signal path compensates for the delay of the chrominance signal through the bandpass filters and the decoders. This ensures that the two signals remain synchronised. [CVI03-2 and 3]

Chroma Processor

The chroma processor generates subcarrier and PAL signals that are locked to the incoming video signal. The subcarrier and PAL signals are used as references by the encoder and main board. The filtered chroma signal derived from the Video 1 input is coupled into pin 1 of the chroma processor chip CA3128 U16. A burst gate signal is derived from the sandcastle pulse by comparator U17 and fed to the CA3128. This burst gate pulse is used internally to lock the subcarrier filter formed by crystal Y6, C147 and associated components to the frequency of the burst from pin 1 of CA3128. Components connected to pins 2, 3, 4, 10, and 11 determine the time constants of the phase-locked loop. A continuous subcarrier signal is available at pin 8 which is converted to TTL levels by Q20. Q22 amplifies the negative-going portion of the PAL signal available at pin 13. This is used to turn on Q21 and thus reset the encoder PAL flip-flop when Q24 is off. Q23 buffers the PAL signal from the encoder U7 and drives Q24 off when the encoder PAL signal is low. Thus the reset pulses from Q22 can only reset the encoder when the encoder PAL pulse is low: this is the out-of-phase condition. The reset pulses are inhibited by Q24 when the encoder PAL pulse is high: the in-phase condition. The reset pulses must be inhibited when in phase since the reset pulse occurs during the burst period and interferes with normal burst phase operation. Q19 generates an adjustable PAL pulse signal level from the encoder PAL pulse to allow subcarrier feedthrough nulling via the R-Y clamp capacitor of the encoder. When no input is connected the crystal oscillator free runs and the PAL reset is disabled. The free running frequency is set by C147. CR20 generates +11.3v from +12v for the chroma processor CA3128.

Decoder 1

Decoder 1 generates red, green and blue (RGB) signals from the composite video 1 input. Synchronisation is taken from the sync separator (4). The decoder output is either the direct RGB signals from RGB input 1 or the RGB signals decoded from composite input 1, depending on the position of SW1/8. In PAL systems a 64uS delay line is required for the decoding operation.

The crystal on U5/26 runs at twice the colour subcarrier frequency. It locks to the external video subcarrier if present or free runs if no video is present.

The RGB outputs from the TDA 3562 are intended to drive the RGB gun drive transistors of a TV set and so have an automatic "black level" control input pin U5/18. Resistors R114,115,116 and 117 are used to maintain the RGB outputs at the correct DC level. The colour saturation control pin U5/5 is bidirectional. When colour video is present it is an input controlled by the SAT. pot RV3, and can be forced low to kill colour by jumper W1. When there is insufficient colour burst on the external video the TDA 3562's colour killer circuit pulls pin 5 low, but it may be forced high by jumper W1 to "unkill" colour.

The output (U5/28) to the 64uS delay line contains chrominance information only. The burst is at a constant level and the level of the picture chrominance is variable, controlled by the saturation input pin U5/5, and the kill/unkill jumper W1.

The inductors L6 and L7 compensate for the capacitance of the input and output piezoelectric transducers on the glass 64uS delay line L5. The balanced output of the delay line is combined with some of the signal from pin U5/28 to produce U and V signals which are fed to pins U5/22 and 23.

Trimpot RV7 together with L6 and L7 adjust the amplitude and phase of the chroma delay circuit. They are adjusted so that correct chroma cancellation occurs on both odd and even lines and does not result in visible "Hanover" bars which are seen as alternate red/green lines on decoded video.

Decoder 2
Decoder 2 generates red, green and blue (RGB) signals from the composite video 2 input. Synchronisation is taken from the sync separator (4). The decoder output is either the direct RGB signals from RGB input 2 or the RGB signals decoded from composite input 2, depending on the position of SW1/7. In PAL systems a 64uS delay line is required for the decoding operation. [U6, TDA 3562, CVI03-3]

Picture controls
The picture controls provide control voltages to the decoders that control the brightness, contrast and saturation of the decoded outputs. If direct RGB inputs are selected to the decoders only the brightness and contrast controls will affect the decoder outputs. [CVI03-4]

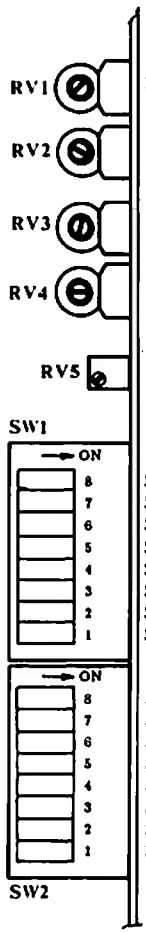
Video source multiplexers
These select the inputs to the digital and analog paths through the CVI. Each path may take its input from the RGB outputs of either Decoder 1 or Decoder 2. The selection is made using two control lines from the digital card, ASEL1 and ASEL2. These TTL signals are buffered to 12V levels by open collector gates U13/11 and 10. When ASEL1 and 2 are low decoder #1 RGB outputs are selected, and when high Decoder #2 outputs are selected. [U8,U9, CVI03-4]

660nS delay lines
These delay lines at the start of the analog path compensate for the delays caused by digitising and processing on the digital path. The delay ensures that picture information sent through the two paths retains horizontal registration. [L14,15,16], (CVI03-4)

Subcarrier phase shifter
The subcarrier phase shifter takes its input from either the external input or the chroma processor, depending on the position of SW1/6, which provides the SUBSEL signal to U1. SW1/5 provides a coarse phase shift of 0 or 180 degrees by selecting the Q or NOT Q outputs of U16/5,12. The subcarrier trimmer RV5 allows fine adjustment by varying the pulse width from the other half of U16. Together these give a full 360 degree range. Transistors Q3A, Q4A and filter L1, C28 and C30 convert the rectangular output of the phase shifter to a constant level sine wave. This is passed to the encoder subcarrier input via RV12 which sets the correct level required by the encoder IC. [U1,U16, CVI03-5]

Encoder
The encoder generates a full composite PAL colour signal from RGB, composite sync and subcarrier inputs. The output (pin 9) can directly drive a 75-ohm cable. The RGB inputs are capacitively coupled. Clamping is done on various signals in the MC1377 using external capacitors C90, C99, C100 and C119. Trimpots RV14 and RV15 vary the DC bias current to the R-Y and B-Y clamp pins and are used to null the amount of residual colour carrier in black. RV13 varies the bias to pin 19 which alters the phase of the R-Y modulator. A PAL null adjustment from the chroma processor via RV20 allows fine nulling of the R-Y modulator on alternate lines. These adjustments require the use of a PAL vectorscope. The MC1377 contains a ramp generator running at horizontal line rate, which is used to set the burst position in the output video and also to trigger the internal PAL flip-flop. The slope of the ramp (and the burst position) is determined by RV11, R130 and C118 connected to U7/1. The PAL flip-flop is reset by the Chroma Processor by pulling pin 20 to ground. U7/16 is an 8.2V reference output voltage used as a stable source for the ramp generator. The PAL phase of the output signal is controlled by the chroma processor and PAL reset circuitry. The bandwidth of the chroma signal generated by the MC1377 is limited by the bandpass circuit (C93, L19, C98) between U7 pins 13 and 10. This delays the chroma by about 350ns and so the luminance must also be delayed by the same amount. This delay is provided by L18 between pins 6 and 8 of U7.

The composite sync signal to U7/2 is derived from the digital board. The subcarrier input U7/17 comes via the phase shifter from either external or internal sources.

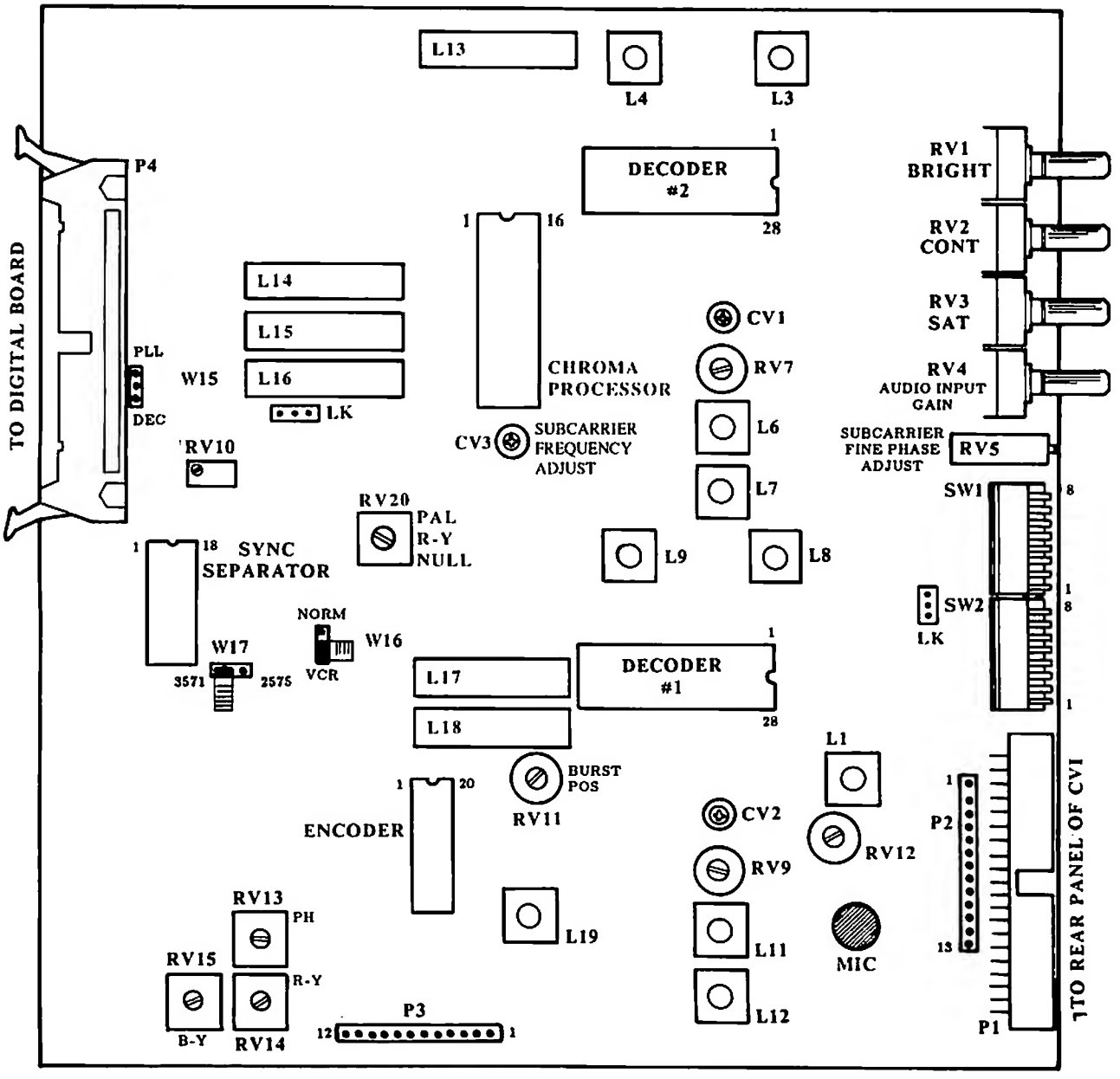


		OFF	ON
SW1/8	Video input 1 source composite	RGB 1	Video 1
SW1/7	Video input 1 source composite	RGB 2	Video 2
SW1/6	Subcarrier source	Ext subc I/P	Internal (1)
SW1/5	Subcarrier phase coarse adj.	0 Degrees	180 deg (2)
SW1/4	Unused	-	
SW1/3	Subcarrier input terminate	-	75 ohms
SW1/2	Stencil input terminate	-	75 ohms
SW1/1	Audio input level range	Low	High
SW2/8	Video 1 Input terminate	-	75 ohms
SW2/7	Video 2 Input terminate	-	75 ohms
SW2/6	Red 1 Input terminate	-	75 ohms
SW2/5	Green 1 Input terminate	-	75 ohms
SW2/4	Blue 1 Input terminate	-	75 ohms
SW2/3	Red 2 Input terminate	-	75 ohms
SW2/2	Green 2 Input terminate	-	75 ohms
SW2/1	Blue 2 Input terminate	-	75 ohms

Notes

(1) The internal subcarrier is both frequency and phase locked to the VIDEO 1 input if a video signal is present on it.

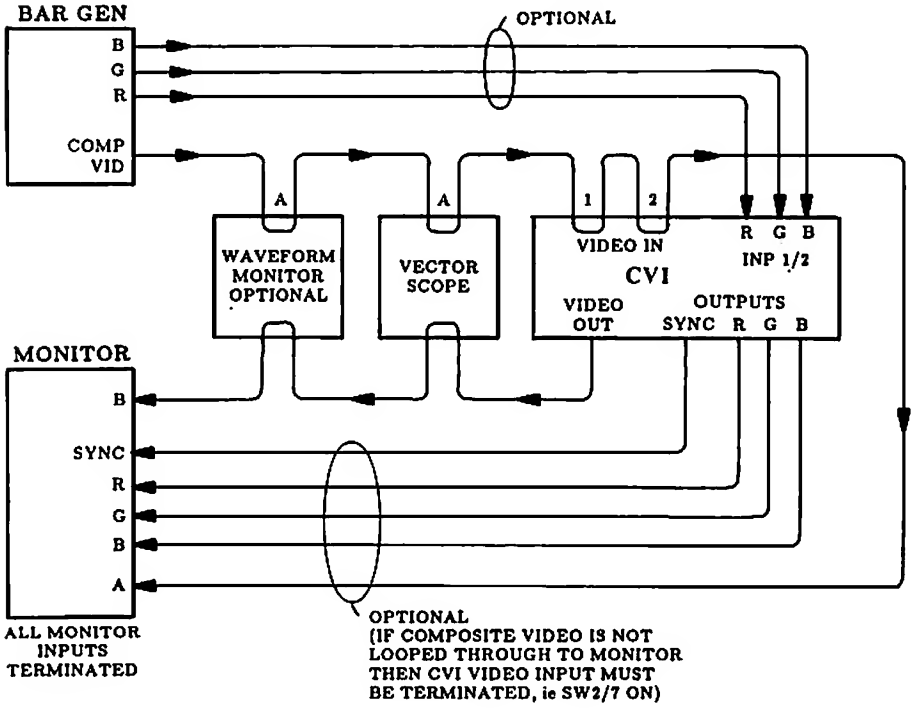
(2) SW1/5 selects a phase shift of zero or 180 degrees. Using it and the phase fine adjustment trimpot, the video output subcarrier phase may be adjusted from 0 degrees to 360 degrees relative to the reference subcarrier.

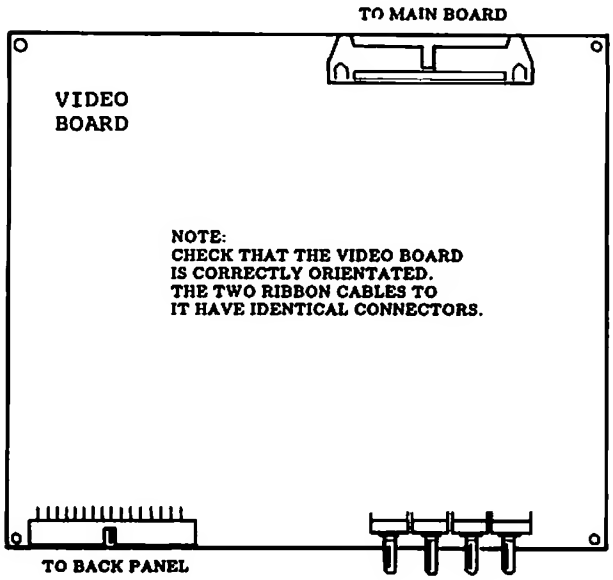

L13
L4
L3
P4
TO DIGITAL BOARD
DECODER #2
1
28
1
16
RV1 BRIGHT
RV2 CONT
RV3 SAT
RV4 AUDIO INPUT GAIN
L14
L15
L16
PLL
W15
DEC
LK
CV1
RV7
CHROMA PROCESSOR
CV3
SUBCARRIER FREQUENCY ADJUST
L6
L7
SUBCARRIER FINE PHASE ADJUST
RV5
RV10
RV20
PAL R-Y NULL
SW1
8
1
SYNC SEPARATOR
18
L9
L8
SW2
LK
NORM
W16
W17
3571
2575
VCR
L17
L18
DECODER #1
28
L1
BURST POS
RV11
ENCODER
20
CV2
RV9
RV12
P2
13
RV13
PH
RV15
R-Y
B-Y
RV14
L19
L11
L12
MIC
P3
12
P1
TO REAR PANEL OF CVI

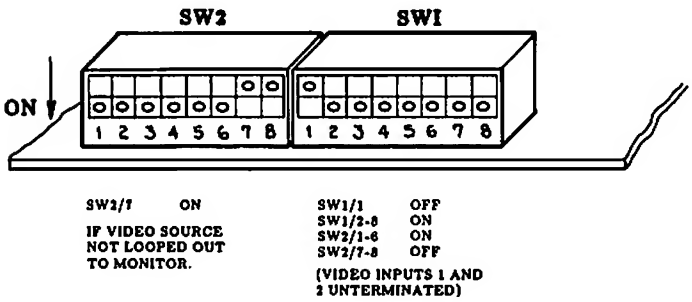
EQUIPMENT REQUIRED

a) 100MHz dual channel C.R.O. (cathode ray oscilloscope).
b) 6 to 7 digit 100MHz frequency meter.
c) PAL Vectorscope (2 inputs).
d) PAL 100% colour bar generator.
e) PAL Composite video monitor with RGB inputs.
f) PAL Waveform monitor (optional).
g) CVI system (main board, front panel, cables, power supply etc.)

GENERAL TEST SETUP & PROCEDURE







SW2/7 ON

IF VIDEO SOURCE
NOT LOOPED OUT
TO MONITOR.

SW1/1 OFF
SW1/2-8 ON
SW2/1-6 ON
SW2/7-8 OFF
(VIDEO INPUTS 1 AND
2 UNTERMINATED)

The diagram above shows original settings of SW1 and SW2

Initial test switch settings on video card
Jumper link settings

W1 - unused
W2 - unused
P2 - unused
P3 - unused
W15 - unused
W16 - VCR
W17 - 3571

General procedure

Due to the interactions between adjustments on the board, the following sequence of operations is recommended:

1) check and adjust sync separator
2) chroma processor
3) set free run frequency of subcarrier crystal
4) check and adjust subcarrier phase shift chain
5) check that main board PLL locks to subcarrier
6) check and adjust video encoder
7) check and adjust decoder #1
8) check and adjust decoder #2
9) check RGB inputs and outputs
10) check audio input

PRESETS USED IN SERVICING

The CVI PRESETS allow the internal state of the CVI to be quickly restored to a predefined condition. For a full description refer to the operation manual.
Only a few of the 100 presets available need to be used while servicing the videoboard. They are:

- 00 Selected at power on, displays the Fairlight logo
- 95 Video 2 through
- 96 Video 1 through
- 97 Internal colour bars

The preset number currently selected is displayed on the front panel LED display. To change the preset number, press the PRESET key followed by two number keys.

For example, **PRESET 9 5** for preset 95.

If the CVI has been in use it is possible that these presets have been changed by the user. In this case reset the above presets. Refer to the "RESET PRESETS" section of the user manual.

The effects and uses of these presets are as follows:

00 At power on, the Fairlight logo is drawn (in colour) in the CVI video RAM and stencil. If video is present on the Video 1 input the CVI locks to it. The Video 1 image is converted to analog RGB by decoder 1, then passed via mux U9 to the analog path on the main board. Simultaneously, the image in the RAM is read out and converted to analog RGB. The RAM image (the logo) and the incoming video are combined by the analog video MUX/MIX and then passed through buffers to the CVI RGB outputs and composite video encoder.
This preset is used while testing the sync separator, main subcarrier oscillator, MUX U9 and the phase shifter circuit.

95 Video input 2 through. The CVI locks to Video 1 input, and passes the Video 2 input through the analog path, i.e. decoder #2, MUX U8, delay lines, main MUX/MIX/buffers, RGB outputs and encoder.
This preset is used to test decoder #2.

96 Video input 1 through. The same as 95, but uses decoder #1.
This preset is used to test decoder #1.

97 Internal colour bars. The CVI locks to Video 1 input if present, but uses the RAM as the sole colour source. The processor writes a "colour bars" image to the RAM. The video route is - RAM, D to A's, MUX/MIX, buffers, encoder.
This preset is used to test and align the encoder.

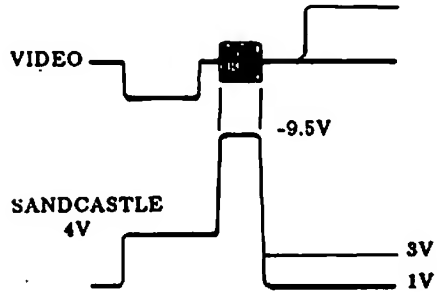
CONTENTS

NOTE:
TTL levels implies a high (or 1) to be above 2.5V and a low (or 0) to be below 0.8V.

Sync separator
IC U12 - TDA 3571B 18 pins

Setup

- Colour bars to Video input #1.
- Ignore CVI controls and video output.
- CRO - sweep 2uS/div.
- CRO - Channel 1 200mV/div. On external video input 1 (P2/5) i.e. Pin 5 of P2.
- CRO - Channel 2 2V/div. On "sandcastle" pulse on U6/7. This comes from U12/15.
- CRO - Trigger on CH1, negative edge of video H sync.



Adjust RV10 so that the sandcastle (CH2) is locked to the video (CH1), with the peak of the sandcastle encompassing the video burst.

Change CRO sweep to 500uS/div. Trigger on vertical sync. Check that the sandcastle signal does not go below 2V during the vertical blanking period.

Check that U11/7 is a TTL low (EXTERNAL SYNC) with video applied to video 1 input. Check that it goes high (INTERNAL SYNC) if video is removed from Video 1 input.

With video applied, check for TTL Horizontal sync pulses on U10/7 and TTL Vertical sync pulses on U13/4.

See page 3.14.1 for block diagram of 3571B.

Chroma Processor

Setup
- Disconnect input to VIDEO 1.
- CRO - sweep 100ns div.
  - CH1 2V div on DEC pin of W15.
  - trigger AC on CH1.
- Frequency meter - DEC pin of W15.
- Vectorscope - reference and sync CHA, NTSC display, input CHB.

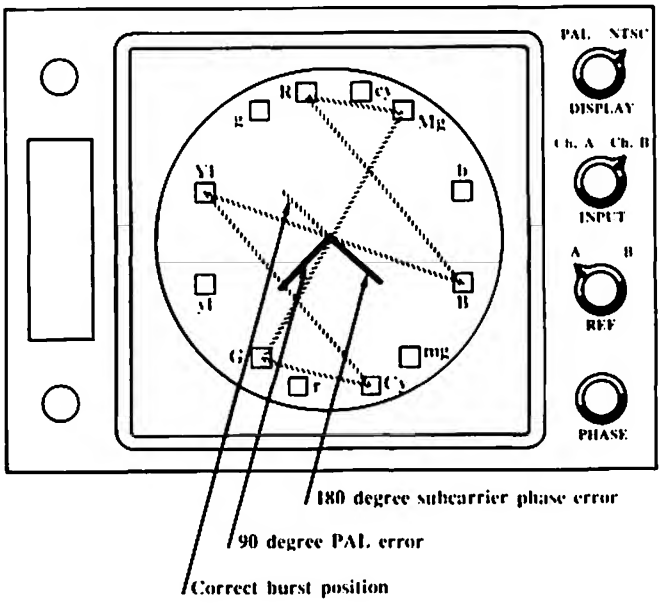
Procedure

Subcarrier Frequency
- The CH1 signal should be a TTL square wave.
- Adjust CV3 (near the chroma processor IC CA3128) so that the subcarrier frequency is 4.433619 MHz +-5Hz.
- Reconnect the video input to VIDEO 1 and check that the frequency at DEC pin of W15 has not changed.
- Disconnect the signal to VIDEO 1 again and check that the frequency is as before. This sets the free-running frequency of the internal subcarrier reference oscillator.

PAL and Subcarrier Phase
(Oscilloscope Method)
- Connect a video signal to VIDEO 1 input.
- Check the signal on pin 20 of the encoder IC U7. This should be a 2Vp-p square wave at half line rate. When the signal to VIDEO 1 is disconnected and reconnected this PAL square wave should be pulled to ground for one or two lines during the burst period after which it should be inhibited.

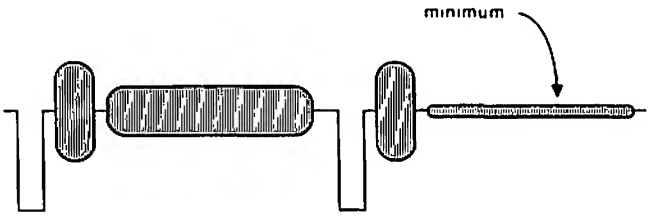
PAL and Subcarrier Phase
(Vectorscope Method)

Assuming that the encoder section is working then the chroma processor can also be checked using the vectorscope.
- Connect a PAL colour bar signal to VIDEO 1 input.
- Select CHB and NTSC display on the vectorscope. See following diagram.

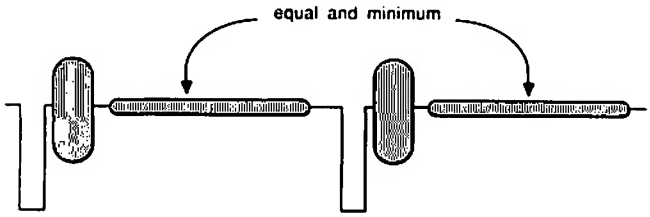


- Align the vectorscope and CVI subcarrier phase so that the burst vectors overlap and are positioned over the top burst mark.
- Disconnect and reconnect the signal to VIDEO 1 several times. The vectorscope display should always revert back to the original display when the signal is reconnected indicating that subcarrier and PAL phase are being recovered correctly from the incoming video.
- With an input to VIDEO 1 turn the CVI off and on several times and again check that the vectorscope display aligns correctly. A 90 degree error could indicate a PAL phase error while a 180 degree error usually indicates a subcarrier phase error.

PAL Null Adjustment
- Clear the screen to black using factory PRESET 3 with the VALUE control set to zero.
- While observing the VIDEO OUT signal on the waveform monitor or CRO adjust RV14 and RV15 to obtain minimum chroma in the picture area on a particular line. See diagram below.



- Adjust RV20 so that any chroma feedthrough on consecutive lines is equal. See diagram below.



- Re-adjust RV14, RV15 and RV20 to obtain minimum chroma feedthrough in the picture area on consecutive lines.
- Select PRESET 97 and check that the colour bar waveforms are the same.

Subcarrier phase shifter

This circuit is used to adjust the phase of the output video subcarrier relative to the input video subcarrier. A full 360 degrees range is possible using the coarse adjust switches and fine adjust trimmer.

The subcarrier source is selected (via U1) from either the external subcarrier input, or the chroma processor. Dual monostables U16 and trimpot RV5 provide the fine phase adjustment. One of the two outputs from U16 (0 or 180 degrees) is selected by U1 and SW1/5 and passed via the subcarrier filter L1 and level control RV12 to the encoder.

Setup

CRO - Sweep 100ns/div
/ - Trigger on CH1
/ - CH1 1V/div, on U1/14 (4053, selectec subcarrier)
/ - CH2 1v/div, on U7/17 (subcarrier input to encoder)

Procedure

To test the external subcarrier input amplifier, connect subcarrier to the input and check that the signal appears on CH1 when SW1/6 is off.

With SW1/6 on, set RV12 to midrange and adjust L1 for maximum amplitude and cleanest waveform at U7/17 (CH2). Next adjust the level pot RV12 for 0.75Vp-p at U7/17. Allowed range is 0.5Vp-p to 1Vp-p.

Check that SW1/5 moves the phase of U7/17 (CH2) by 180 degrees relative to U1/14 (CH1), and that Rv5 also varies the phase.

Alternatively, if the rest of the board is working, supply colour bars to input 1, synchronise the vectorscope to the bar generator, select Preset 97 and view the CVI output on the vectorscope. Check that the CVI output burst can be rotated through 360 degrees using the coarse and fine phase controls.

Subcarrier locking

Setup

- CRO - sweep 100nS/div.
- CRO - CH1 2V/div. on DEC pin of W15.
- CRO - CH2 2V/div. on PLL pin of W15.
- CRO - trigger on CH1.
- Colour bars to Video 1 input.

The signal on CH2 should be a TTL square wave at the same frequency of CH1, and in steady phase lock.

RGB, sync and stencil outputs

The RGB lines come directly from the main board, while the SYNC and STENCIL signals are generated on the main board and buffered by U13 on the video board.

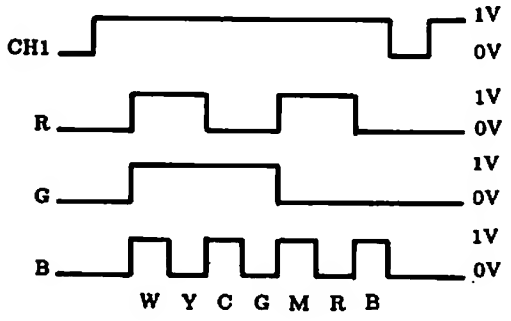
Check these before proceeding to the encoder.

Setup

- Select preset 97 (internal colour bars)
- If your monitor has RGB inputs, connect the CVI's RGB and SYNC outputs to the monitor.

Check for a clean and correct colour bars image.

Check for signals as indicated below:



Otherwise -

- CRO - Sweep 10uS/division.
- CRO - CH1 0.5V/division. On SYNC OUT signal (with 75 ohm termination).
- CRO - CH2 0.5V/division. On R/G/B signal out (with 75 ohm terminations).
- CRO - Trigger on CH1, TV H sync.

Check for signals as indicated below:

Turn the CVI OFF. Wait for 5 or more seconds and turn ON, to obtain the startup logo. Check that the STENCIL output is 1V p-p into 75 ohms. The signal will not be regular or coherent except during sync and blanking.

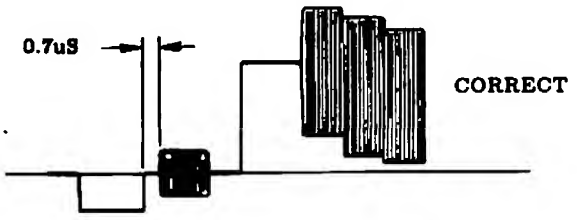
Video encoder

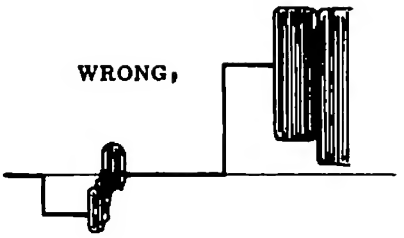
The PAL encoder IC U7 takes RGB, subcarrier and sync inputs and generates composite colour video.

Setup

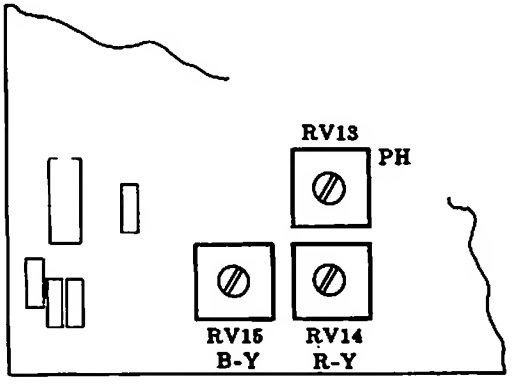
- Preset 97 (internal colour bars).
- Select the CVI composite video output on the monitor, vectorscope and waveform monitor or CRO.

Adjust RV11 for correct colour burst position on the front porch as indicated below.





Adjust "PH" pot for symmetrical vector display (U7/19).
Adjust "R-Y" (U7/12) and "B-Y" (U7/11) pots for minimum chroma on sync and front and back porches. Alternatively adjust these pots so that the central point of the vector display is centred on the grid.



Check the colour bars on the monitor for correct colour and hue.

Decoder #1 and #2 - TDA 3562

The PAL decoder IC's U5 and U6 convert composite colour video to analog RGB signals. They require a multilevel "sandcastle" sync input signal for burst sampling, H syncs, etc. The external RGB inputs are processed and switched by the decoders also.

Refer to the TDA 3562A block diagram on page 3.14

General Decoder Setup

View CVI RGB outputs on monitor. Alternatively, view CVI composite video out.

- 100% Colour bars to input 1 and 2.
- Brightness to minimum, saturation to mid range, contrast to maximum.
- CRO - Sweep 10uS/division.
- CRO - CH1 0.5V/division on Video 1 input.
- CRO - Trigger on CH1, TV horizontal.

Decoder #1 setup

- Preset 96 (video 1 through).
- Set RV7 (amplitude adjust) fully anticlockwise.
- CRO - CH2 0.5V/division

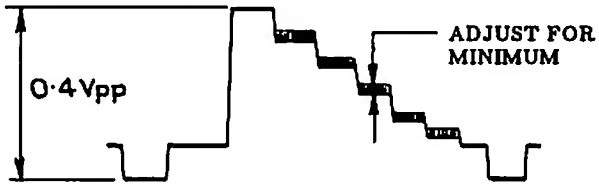
Short pins 24 and 25 of U5 together. This disables the voltage control of the crystal oscillator and allows the free run frequency to be adjusted.

Adjust CV1 to the middle of the range in which colour appears on the screen. Remove the input to video 1 then put it back, checking that colour reappears when it is replaced. If not, readjust CV1.

Connect CH2 to U5/4. Adjust L3 for maximum chroma amplitude.

Connect CH2 to U5/8. Adjust L4 for minimum chroma on the luminance signal.

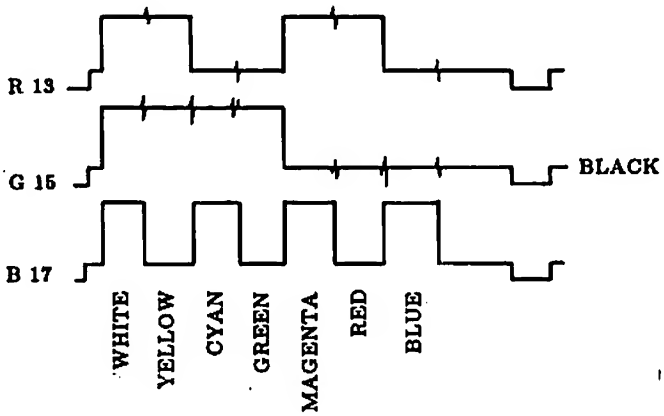
Connect CH2 to U5/8. Adjust L4 for minimum chroma on the luminance signal.



CRO - CH2 2V/division. On U5 pins 13,15,17 alternatively.

Adjust L6, L7 and RV7 for the best "RGB bars" waveforms on U5 pins 13, 15 and 17.

i.e., U5 pin



The aim is to get the tops and black levels of each waveform all lined up (equal levels). Pin 17 (blue) is the most critically affected by RV7. "Twitter" or alternate line flickering of each of the traces should be minimised since this causes Hanover bars on the screen (alternate red and green lines).

Several iterations may be required to get the best results.

Brightness and saturation controls also affect these waveforms.

Decoder #2 setup

- Preset 95 (video 2 through).
- Set RV9 (amplitude adjust) fully anticlockwise.
- CRO - CH2 0.5V/division.

Short pins 24 and 25 of U6 together. This disables the voltage control of the crystal oscillator and allows the free run frequency to be adjusted.

Adjust CV2 to the middle of the range in which colour appears on the screen. Remove the input to video 2 then put it back, checking that colour reappears when it is replaced. If not, readjust CV2.

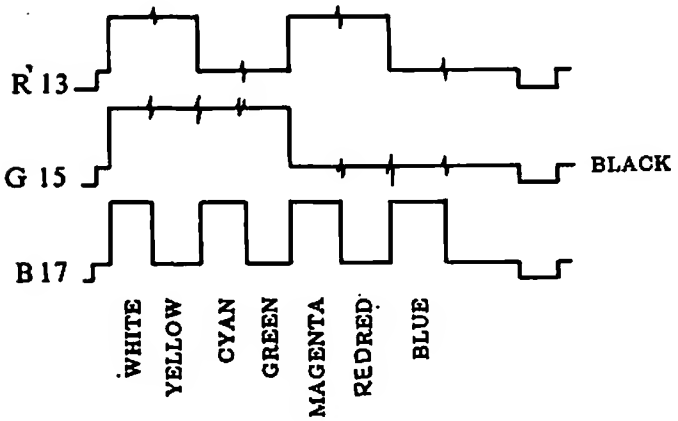
Connect CH2 to U6/4. Adjust L8 for maximum chroma amplitude.

Connect CH2 to U6/8. Adjust L9 for minimum chroma on the luminance signal.

CRO - CH2 2V/division. On U6 pins 13,15,17 alternatively.

Adjust L11, L12 and RV9 for the best RGB bars waveforms on U6 pins 13, 15 and 17.

i.e., U6 pin



The aim is to get the tops and black levels of each waveform all lined up (equal levels). Pin 17 (blue) is the most critically affected by RV9. "Twitter" or alternate line flickering of each of the traces should be minimised since this causes Hanover bars on the screen (alternate red and green lines).

Several iterations may be required to get the best results.

RGB inputs

These are analog RGB inputs to the decoder chips U5 and U6. SW1/8 and SW1/7 select either RGB or composite on decoder #1 (U5) and decoder #2 (U6) respectively. See VIDEO BOARD OPERATING CONTROLS page 3.3.

To check RGB 1 inputs -

View CVI composite or RGB video output on monitor.
Select preset 96 (Video 1 through).
Apply colour bars to video 1 input.
Turn SW1/8 OFF. The colour bar output from the CVI should disappear (become black).
If the bar generator has RGB outputs, connect them to the CVI RGB 1 inputs and check for correct bars output from the CVI.

Otherwise, loop the composite video bars signal through to the RGB 1 inputs one at a time and check for R,G and B images out of the CVI. Note that there should be only one termination on the video input, so the video input should be unterminated and the RGB inputs terminated.

To check RGB 2 inputs -

Select preset 95. (Video 2 through)
Apply colour bars to Video 1 and loop through to Video 2.
(Only terminate Video 2.)
Turn video board switch 1/7 OFF. The colour bar output from the CVI should disappear (become black).
Apply RGB bars or composite video to the RGB 2 inputs while observing the CVI output as for the decoder #1 procedure above.

Audio input

The audio input circuit consists of op amp U2 with a high or low gain selected by SW1/1, followed by the sensitivity pot RV4. The internal microphone or an external line level input are selected automatically by the external input socket. The signal is passed to a peak detector, a low pass filter, a band pass filter and a high pass filter, giving Envelope, Bass, Mid and Treble signals. These are sent to the multiplexer on the front panel to be digitised.

The audio analyser can be tested either by observation on a CRO, or by use of the CVI Testing ROM software (see your distributor).

Setup

- Set the audio sensitivity pot RV4 to 3/4 (clockwise).
- Set SW1/1 ON.

Quick check

Using either an external microphone plugged into the AUDIO INPUT jack on the back of the CVI, or the internal microphone MIC1 on the video board, check that sounds picked up by the microphone affect the voltage levels at the test points on the video board.

Connect a line level (200mV pp or greater) music source to the external input jack. Adjust the audio sensitivity pot RV4 for optimum response.

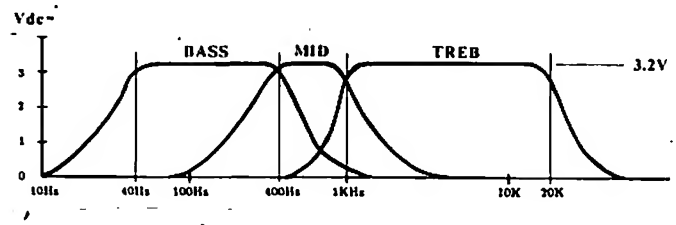
Detailed check

Equipment required

Audio oscillator
DC voltmeter
Oscilloscope

Setup

- Disconnect the back plane to video board ribbon cable from P1 on the video board.
- Connect the audio oscillator sine wave output to the video card AUD input at P2/7 and adjust the level to 1V pp (keep constant for all measurements).
- Set SW/1 on.
- Adjust the SENS pot RV4 for 7V pp at U4/14 (just less than the level at which the signal clips on the positive peaks) with a 1kHz input signal.
- While varying the input frequency and observing the DC voltages at the BASS, MID and TREB test points, check that the filter characteristics are approximately as follows.



Operating adjustments

These consist of the five pots and sixteen switches on the edge of the video board.

To adjust the video control pots -

Select Preset 96
Connect colour bars to Video input 1
View the output of the CVI on the monitor
Flip between Presets 96 (external video) and Preset 97 (internal bars).
Adjust the Brightness, Contrast and Colour Saturation controls so that the CVI internal colour values (Preset 97) match the external video range (Preset 96). For example, the two white values should be equally bright, etc. This may have to be adjusted for various source material.

The video/RGB/stencil and subcarrier termination switches should be set ON for the signal cables that terminate at the CVI, and OFF for those that are looped through the CVI.

The fine phase adjust and audio sensitivity pots are set depending on the installation.

Notes 1. The tests for each section should be carried out in the CVI Preset indicated.

2. The components to be adjusted in each test are indicated in square brackets.

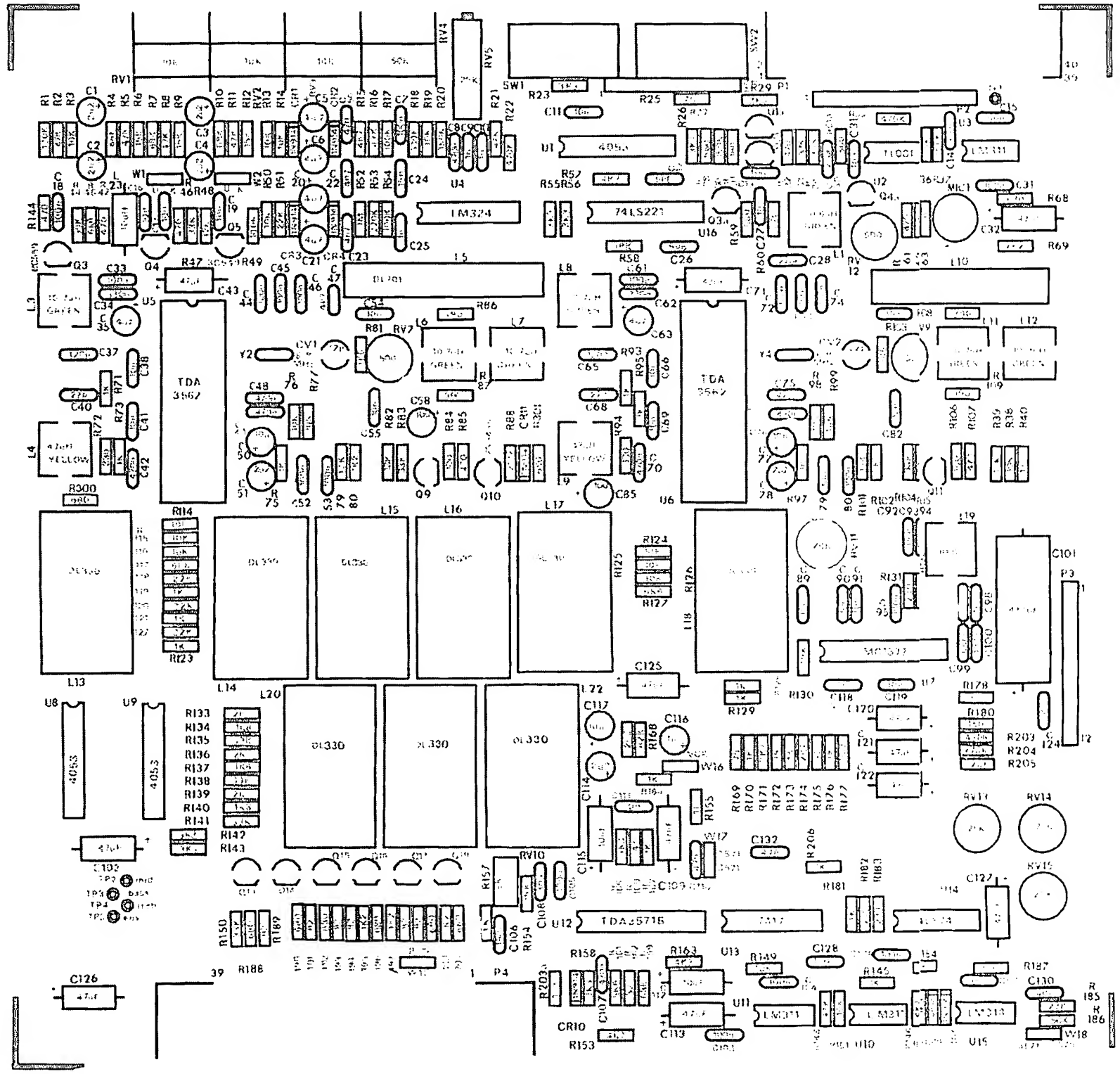
TEST	TEST POINT	EQUIPMENT
SETUP Set DIP switches. Set jumper links.		
SYNC (Preset 00) Check against video input: - sandcastle position and levels [RV10] - EXTSYNC signal - horizontal sync signal - vertical sync signal	 U6/7 U11/7 U10/7 U13/4	
SUBCARRIER (Preset 00) Check: - Subcarrier amplifier output > 2.5V - Subcar. oscillator free run frequency PAL 8.867238 MHz [CV1] - PLL lock - External subcarrier input amp. [SW1/6] - Subcarrier filter [RV12,L1] - Subcarrier level [RV12] - Subcarrier phase shift [SW1/5,RV5]	 W15 (DEC) W15 (DEC) (W15) DEC vs U14/9 U1/14 U7/17 U7/17	 Vectorscope
RGB OUTPUTS AND STENCIL (Preset 00) Check.		CRO or RGB Monitor
ENCODER (Preset 97) Adjust: - Burst position [RV11] - Chroma filter [L19] - Chroma balance [RV13,RV14,RV15]	 	 CRO Vectorscope Vectorscope
DECODER 1 (Preset 96) Adjust: - Maximum chroma [L3] - Minimum chroma [L4] - PAL : RGB bars [L6,L7,RV7]	 U4/4 U4/8 U4/13,15,17	 Monitor
DECODER 2 (Preset 95) Adjust: - Maximum chroma [L8] - Minimum chroma [L9] - PAL : RGB bars [L11,L12,RV9]	 U5/4 U5/8 U6/13,15,17	 Monitor
RGB INPUTS 1 & 2 (Presets 96 & 95) Check.		 Monitor
AUDIO INPUT Check. [SW2/1,RV4]		 Monitor
COLOUR LEVELS (Presets 96 and 97) Adjust: [RV1,RV2,RV3]		 Monitor

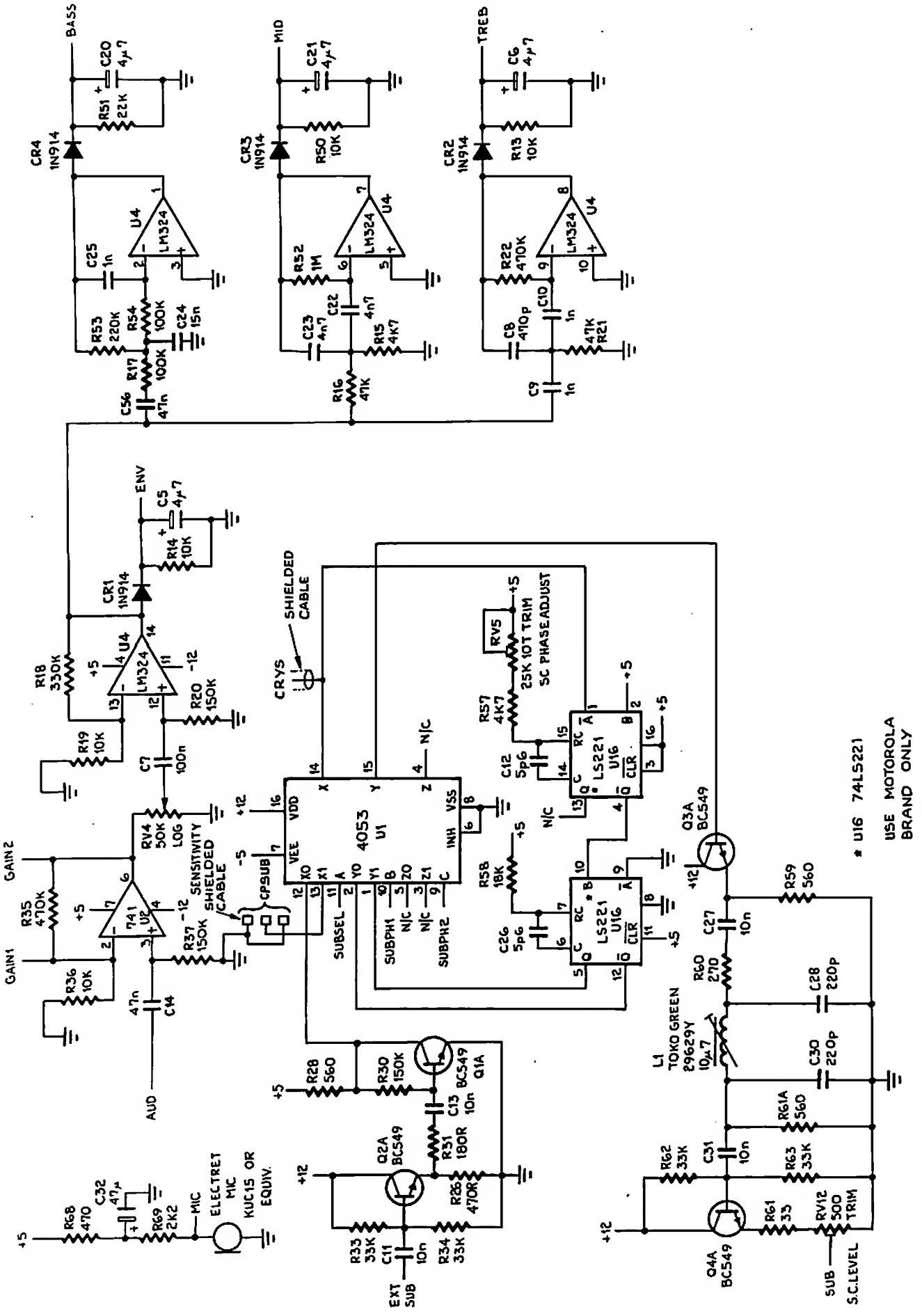
1) Loss of colour on output in internal sync mode (no external video).
- Decoder #1 XTAL OSC free run frequency wrong (not 2 x Fsc)
- Move W15 to DEC position. If colour returns then main board PLL is not locking to video subcarrier.
- Divider U14 or phase shift chain faulty. Check that the encoder is getting subcarrier.
- Burst is in the wrong position.

2) Loss of colour on composite input.
- Decoder XTAL OSC free run frequency wrong.
- link W1 or W2 set in U position.
- saturation control RV3 set too low.

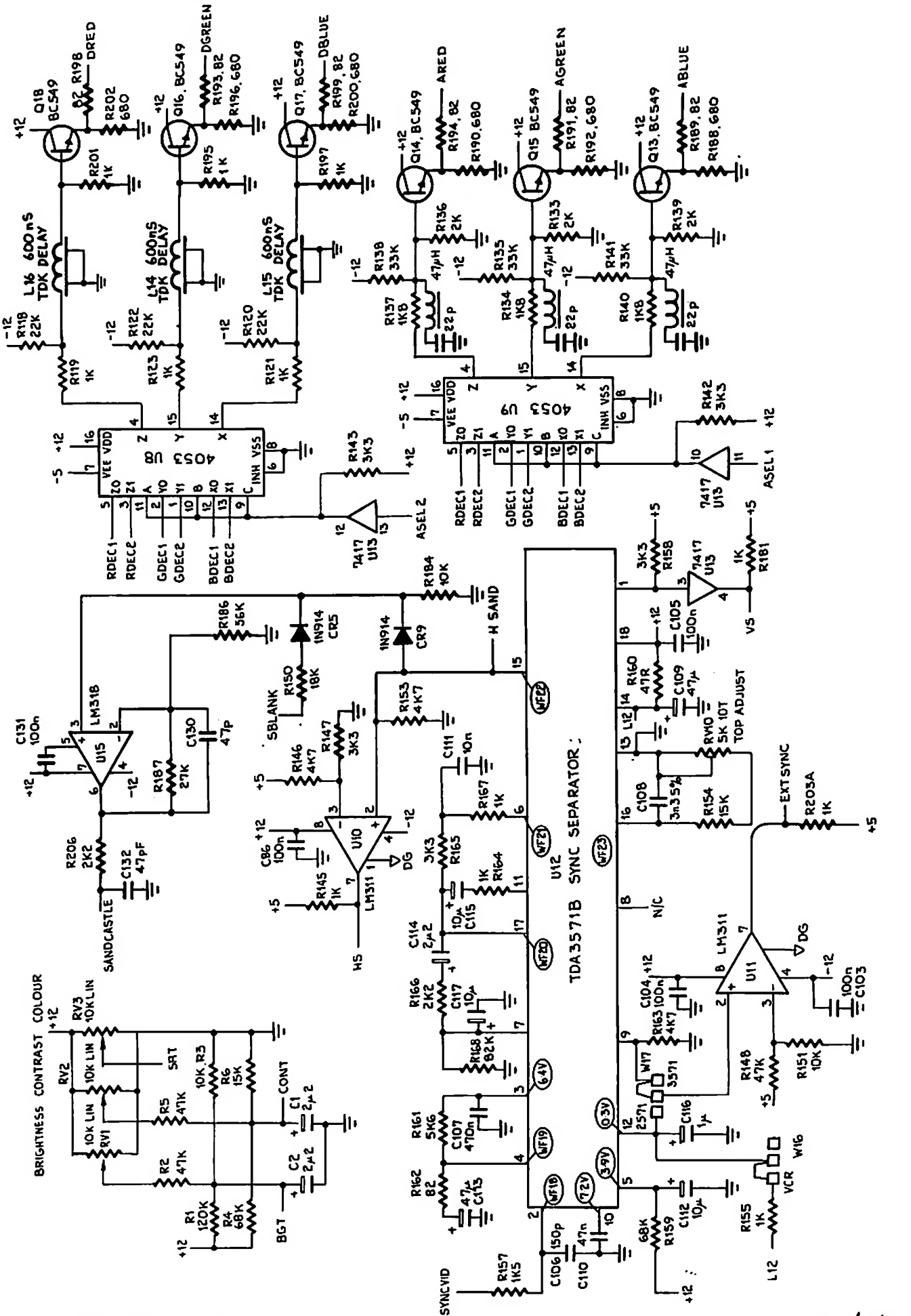
3) Screen tears and rolls.
- EXTSYNC signal is low when no input video to VIDEO 1.
- Vs or Hs signals are missing when in external sync.

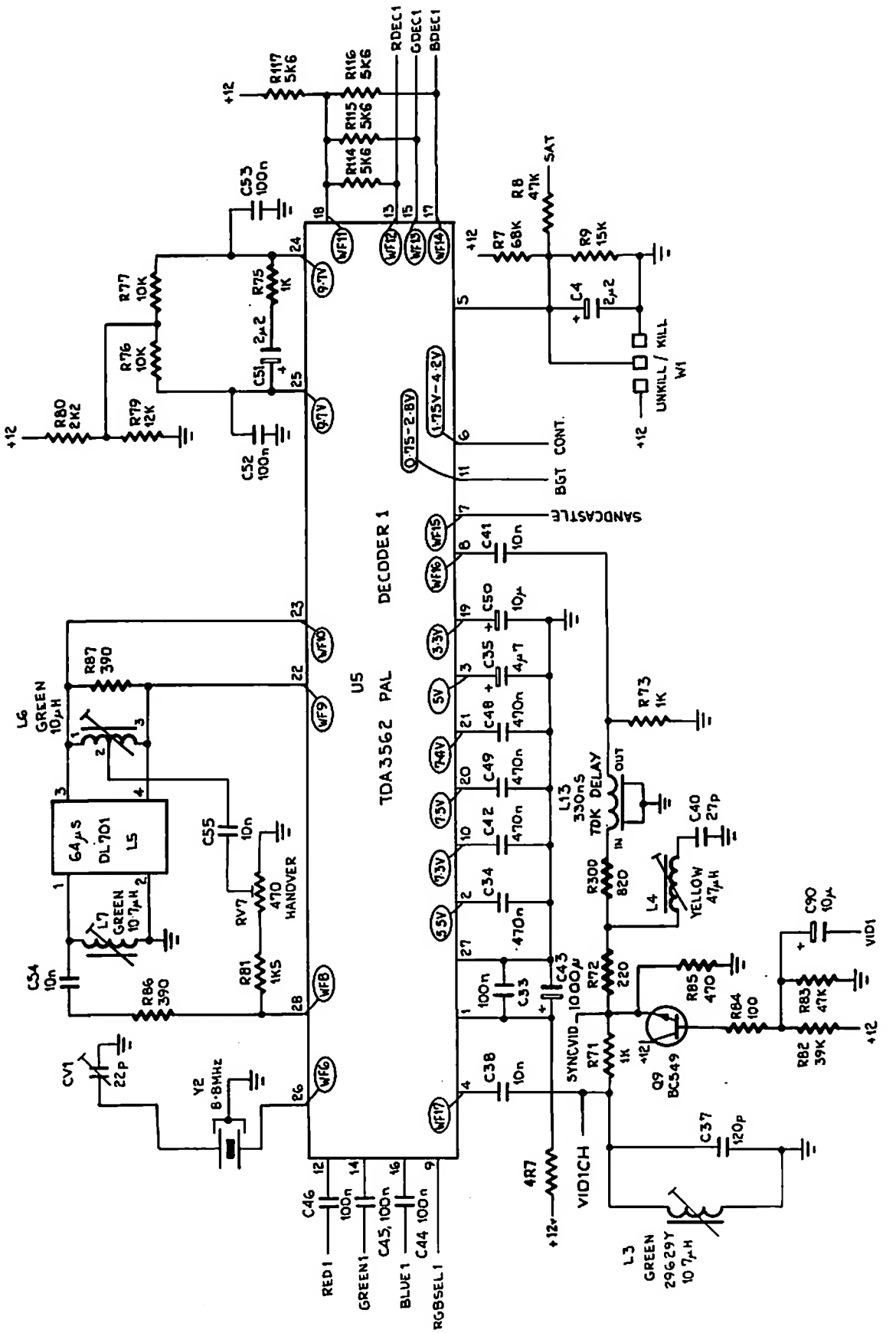
COMPONENT OVERLAY

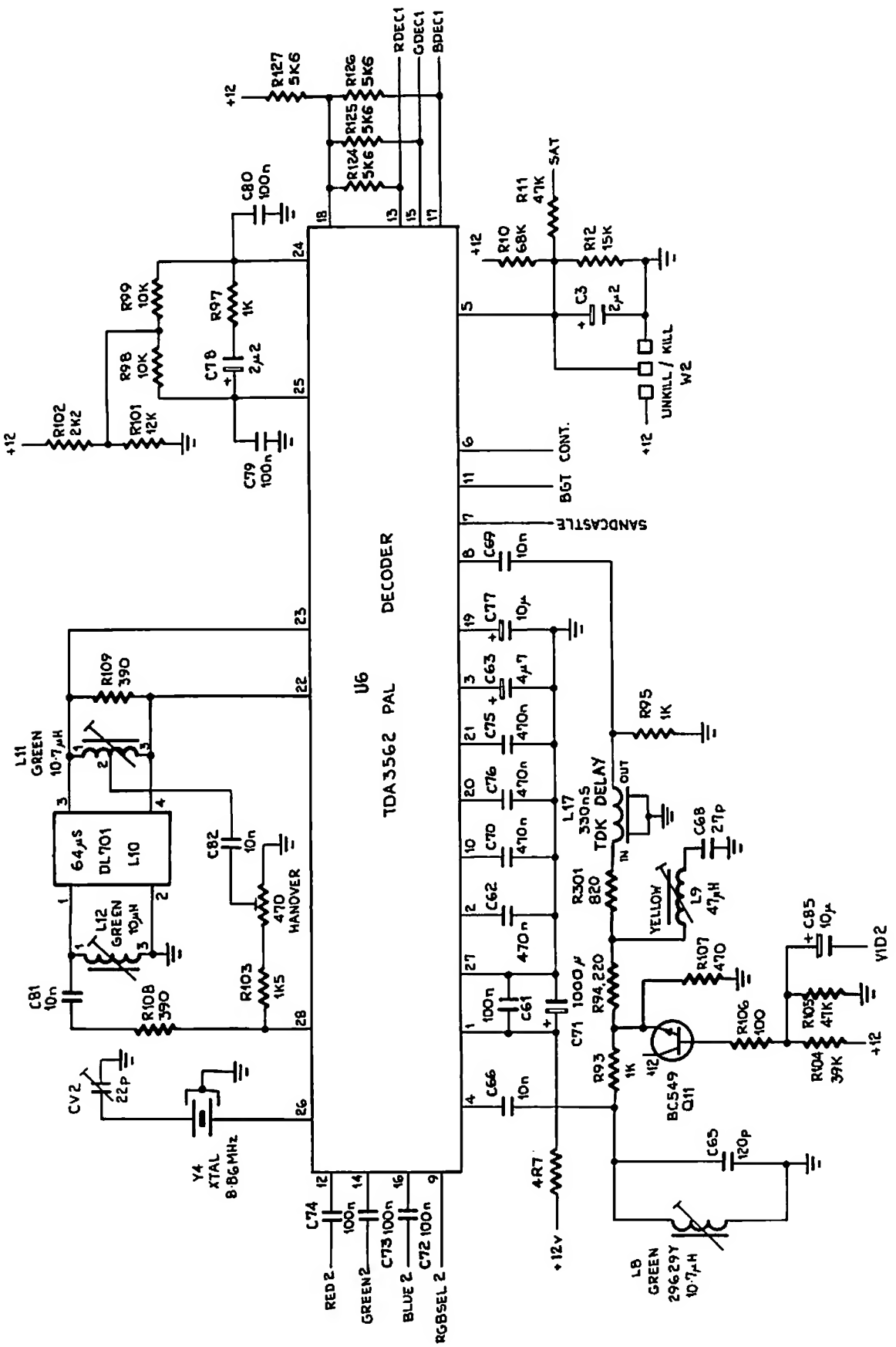


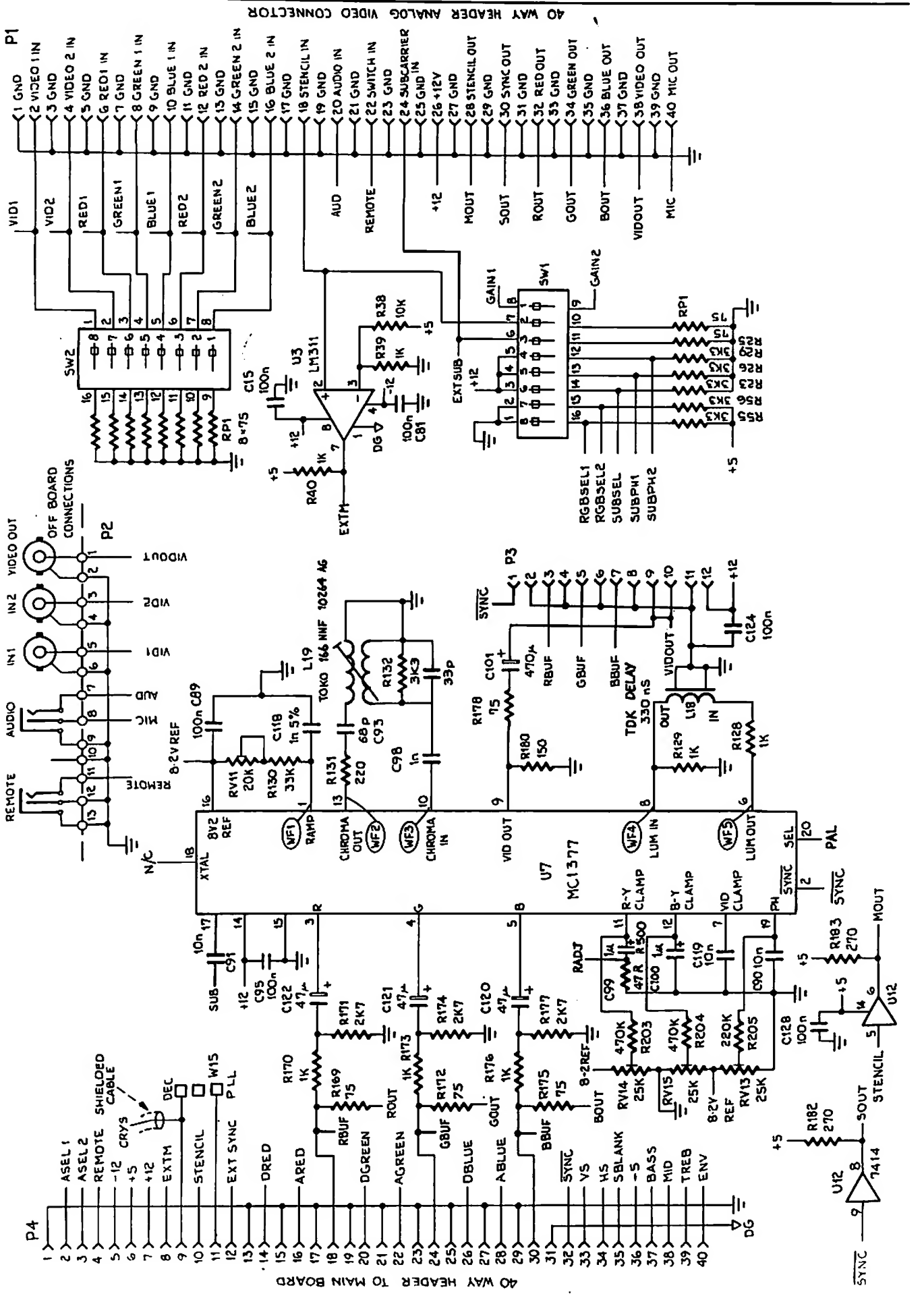

BASS
MID
TREB
ENV
CR1 1N914
CR2 1N914
CR3 1N914
CR4 1N914
U4 LM324
U1 4053
U2 741
U16 74LS221
SHIELDED CABLE
CRYS
SENSITIVITY
SC PHASE ADJUST
TOKO GREEN 29629Y
ELECTRET MIC KUC15 OR EQUIV.
EXT SUB
SUB S.C.LEVEL
* U16 74LS221 USE MOTOROLA BRAND ONLY

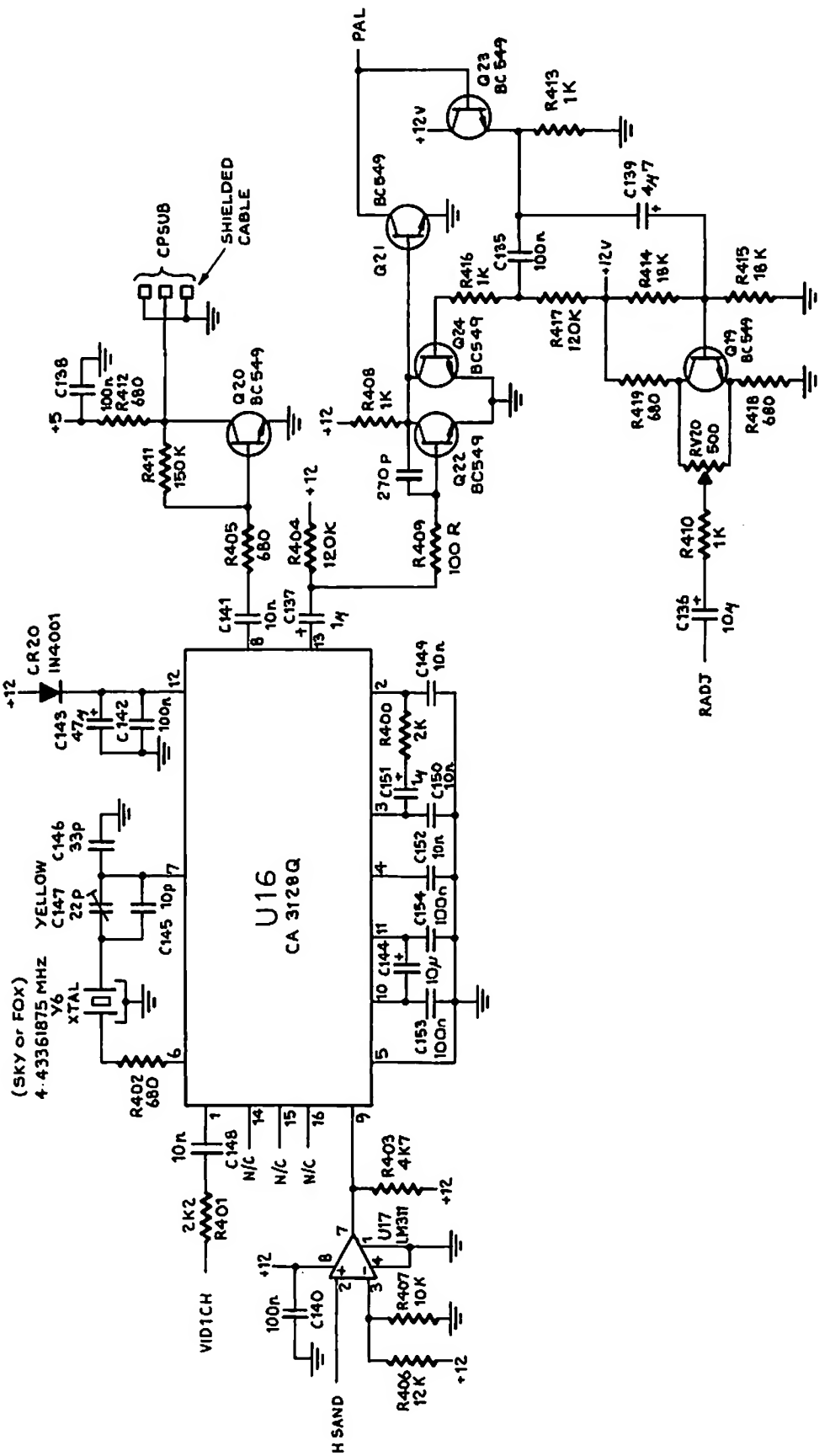
PAL SYNC SEPARATOR VIDEO MULTIPLEXER

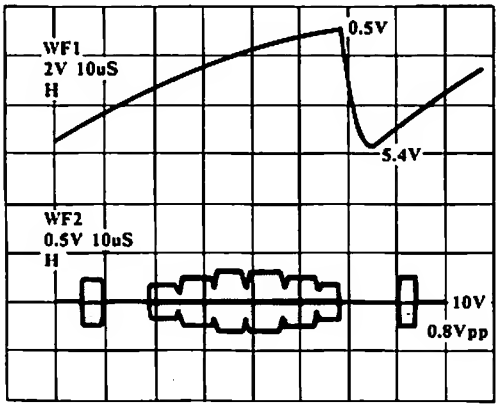


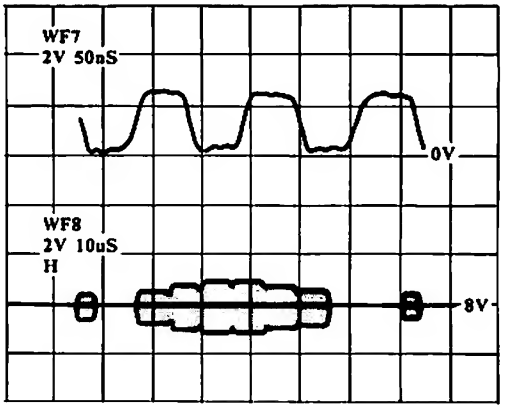

U5
TDA3562 PAL DECODER 1
SANDCASTLE
BGT CONT.
UNKILL / KILL
W1
SAT
L6 GREEN 10µH
L7 GREEN 10·7µH
L5 64µs DL701
L13 330nS TDK DELAY
L4 YELLOW 47µH
L3 GREEN 29629Y 10·7µH
RV7 470 HANDOVER
Y2 8·8MHz
Q9 BC549
SYNCVID
VIDICH
RED1
GREEN1
BLUE1
RGBSEL1
VID1
+12
+12v

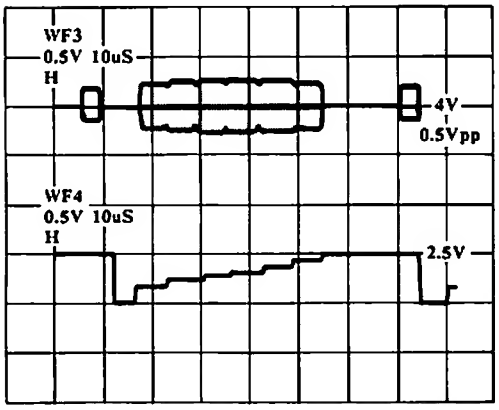

U6
TDA3562 PAL DECODER
+12
R127 5K6
R126 5K6
R125 5K6
R124 5K6
RDEC1
GDEC1
BDEC1
C80 100n
R99 10K
R98 10K
R97 1K
C78 2µ2
R102 2K2
R101 12K
C79 100n
R10 68K
R11 47K SAT
R12 15K
C3 2µ2
UNKILL / KILL W2
BGT CONT.
SANDCASTLE
C69 10n
C77 10µ
C63 4µ7
C75 470n
C76 470n
C70 470n
C62 470n
C61 100n
C66 10n
R95 1K
L17 330nS TDK DELAY
C68 27p
L9 47µH
YELLOW
R301 820
R94 220
C71 1000µ
R107 470
R106 100
R105 47K
R104 39K
C85 10µ
VID2
BC549 Q11
R93 1K
4R7
+12v
C65 120p
L8 GREEN 296297Y 10·7µH
L11 GREEN 10·7µH
64µS DL701 L10
L12 GREEN 10µH
C82 10n
470 HANOVER
R103 1K5
C81 10n
R108 390
R109 390
CV2 22p
Y4 XTAL 8·86MHz
C74 100n
C73 100n
C72 100n
RED 2
GREEN 2
BLUE 2
RGBSEL 2

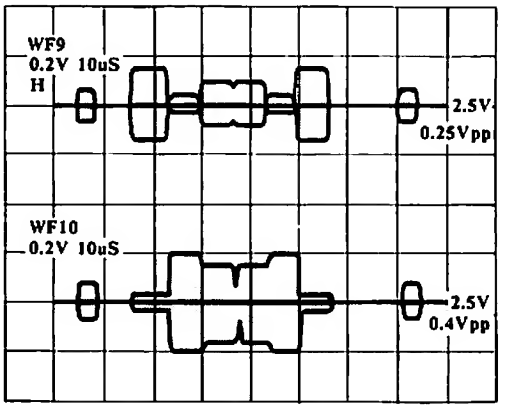

40 WAY HEADER ANALOG VIDEO CONNECTOR
P1
1 GND
2 VIDEO 1 IN
3 GND
4 VIDEO 2 IN
5 GND
6 RED 1 IN
7 GND
8 GREEN 1 IN
9 GND
10 BLUE 1 IN
11 GND
12 RED 2 IN
13 GND
14 GREEN 2 IN
15 GND
16 BLUE 2 IN
17 GND
18 STENCIL IN
19 GND
20 AUDIO IN
21 GND
22 SWITCH IN
23 GND
24 SUBCARRIER
25 GND IN
26 +12V
27 GND
28 STENCIL OUT
29 GND
30 SYNC OUT
31 GND
32 RED OUT
33 GND
34 GREEN OUT
35 GND
36 BLUE OUT
37 GND
38 VIDEO OUT
39 GND
40 MIC OUT
VID1
VID2
RED1
GREEN1
BLUE1
RED2
GREEN2
BLUE2
AUD
REMOTE
+12
MOUT
SOUT
ROUT
GOUT
BOUT
VIDOUT
MIC
SW2
RP1
8-75
C15
100n
U3
LM1311
R38
10K
R39
1K
-12
C81
100n
DG
R40
1K
EXTM
EXT SUB
GAIN1
GAIN2
SW1
RGBSEL1
RGBSEL2
SUBSEL
SUBPH1
SUBPH2
OFF BOARD CONNECTIONS
P2
VIDEO OUT
VIDOUT
VID2
VID1
AUD
MIC
REMOTE
N/C
P3
SYNC
C124
100n
C101
470µ
RBUF
GBUF
BBUF
VIDOUT
TDK DELAY
330 nS
R178
75
R180
150
R129
1K
R128
1K
L18
L19
TOKO 166 NNF 10264 AG
R132
3K3
33p
C89
100n
8-2V REF
RV11
20K
C118
1n 5%
R130
33K
R131
220
68p
C93
C98
1n
WF1
RAMP
WF2
CHROMA OUT
WF3
CHROMA IN
WF4
LUM IN
WF5
LUM OUT
U7
MC1377
XTAL
8V2 REF
VID OUT
SEL
PAL
R-Y CLAMP
B-Y CLAMP
VID CLAMP
PH
SYNC
R183
270
MOUT
U12
7414
R182
270
SOUT
STENCIL
C128
100n
RADJ
47R
R500
C100
C99
C119
10n
C90
10n
R203
470K
R204
470K
R205
220K
RV14
25K
RV15
25K
RV13
25K
8-2V REF
8-2REF
BOUT
R169
75
R172
75
R175
75
R170
1K
R173
1K
R176
1K
R171
2K7
R174
2K7
R177
2K7
C121
47µ
C120
47µ
C122
47µ
C95
100n
C91
10n
SUB
+12
SHIELDED CABLE
CRYS
DEC
W15
PLL
EXT SYNC
P4
ASEL 1
ASEL 2
REMOTE
-12
+5
+12
EXTM
STENCIL
DRED
ARED
DGREEN
AGREEN
DBLUE
ABLUE
SYNC
VS
HS
SBLANK
-5
BASS
MID
TREB
ENV
DG
40 WAY HEADER TO MAIN BOARD

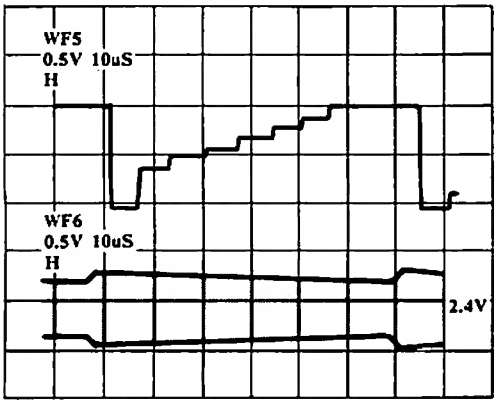

PAL
Q23 BC549
+12V
R413 1K
BC549
Q21
C139 4µ7
C135 100n
R416 1K
+12V
R414 18K
R415 18K
R417 120K
Q24 BC549
Q19 BC549
R419 680
R418 680
RV20 500
R410 1K
C136 10µ
RADJ
CPSUB
SHIELDED CABLE
C138 100n
R412 680
+5
Q20 BC549
R411 150K
+12
R408 1K
270P
Q22 BC549
R409 100R
R405 680
R404 120K
+12
C141 10n
C137 1µ
CR20 IN4001
+12
C143 47µ
C142 100n
C149 10n
R400 2K
C151 1µ
C150 10n
C152 10n
C154 100n
C144 10µ
C153 100n
C146 33P
YELLOW
C147 22P
C145 10p
(SKY or FOX) 4·43361875 MHz
Y6 XTAL
R402 680
U16
CA 3128Q
10n C148
N/C
N/C
N/C
R403 4K7
+12
2K2 R401
VID1CH
U17 LM311
+12
100n C140
R407 10K
R406 12K
+12
H SAND

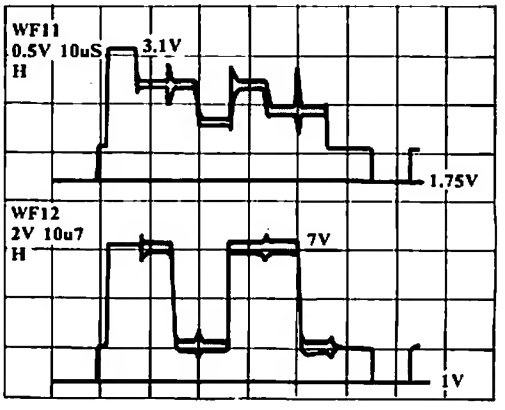

WF1
2V 10uS
H
0.5V
5.4V
WF2
0.5V 10uS
H
10V
0.8Vpp

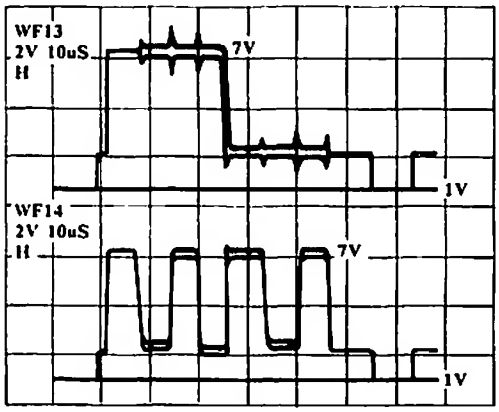

WF7
2V 50nS
0V
WF8
2V 10uS
H
8V

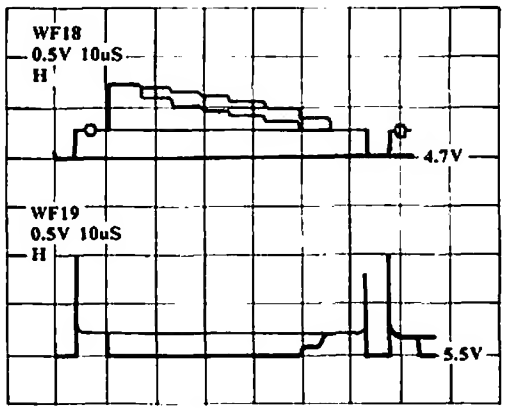

WF3
0.5V 10uS
H
4V
0.5Vpp
WF4
0.5V 10uS
H
2.5V

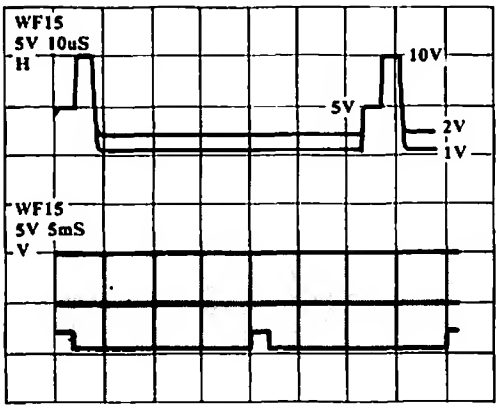

WF9
0.2V 10uS
H
2.5V
0.25Vpp
WF10
0.2V 10uS
2.5V
0.4Vpp

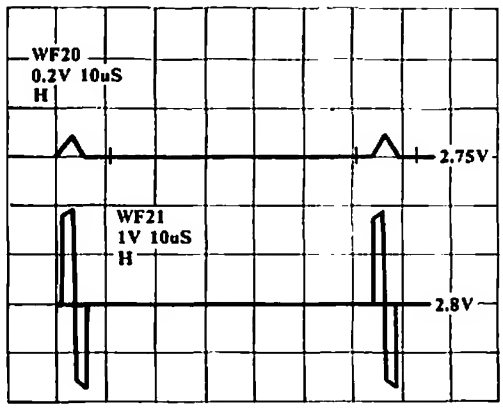

WF5
0.5V 10uS
H
WF6
0.5V 10uS
H
2.4V

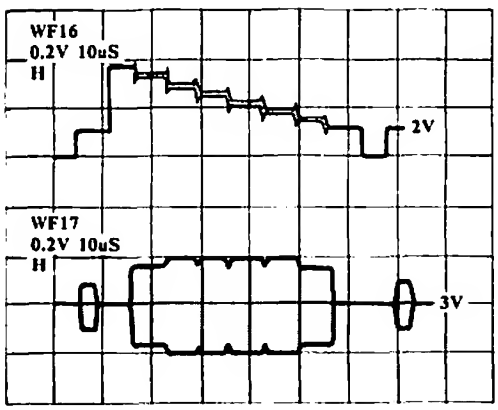

WF11
0.5V 10uS
H
3.1V
1.75V
WF12
2V 10u7
H
7V
1V

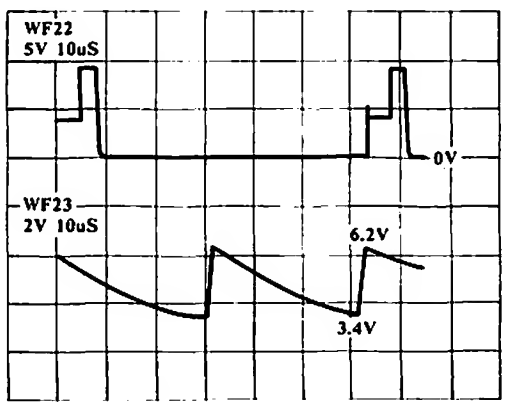

WF13
2V 10uS
H
7V
1V
WF14
2V 10uS
H
7V
1V


WF18
0.5V 10uS
H
4.7V
WF19
0.5V 10uS
H
5.5V

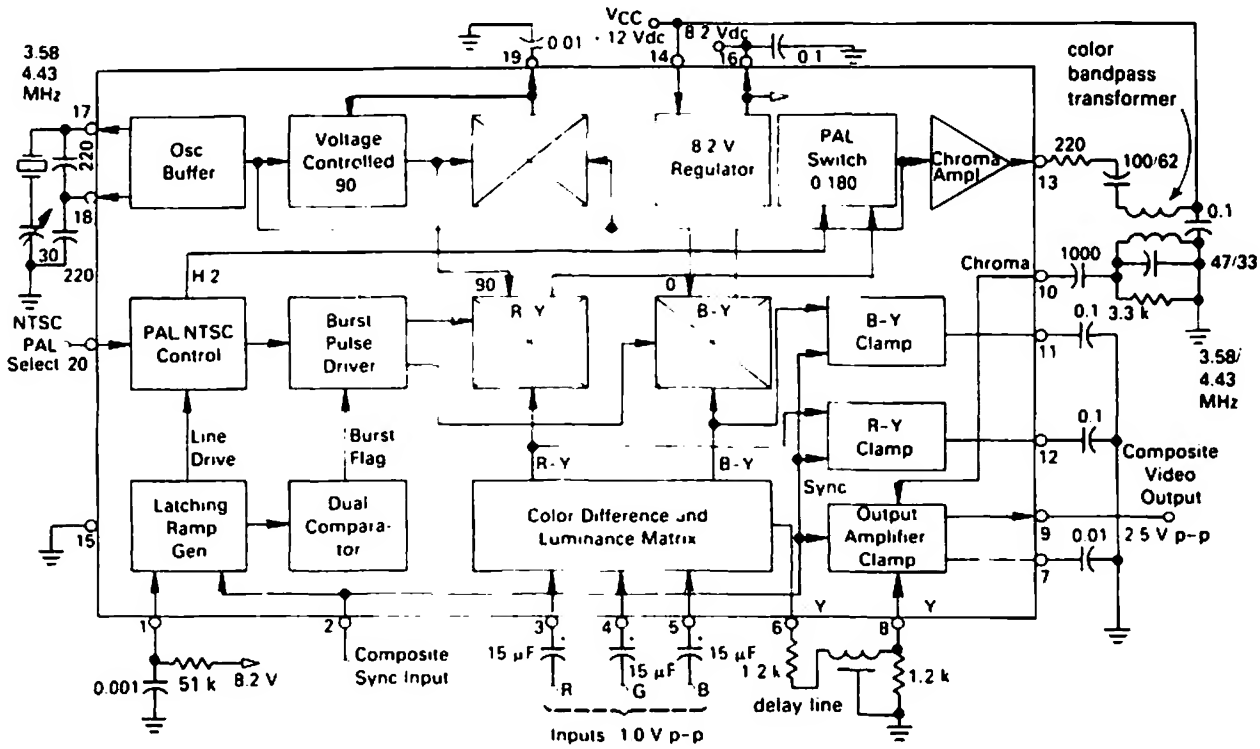

WF15
5V 10uS
H
10V
5V
2V
1V
WF15
5V 5mS
V


WF20
0.2V 10uS
H
2.75V
WF21
1V 10uS
H
2.8V

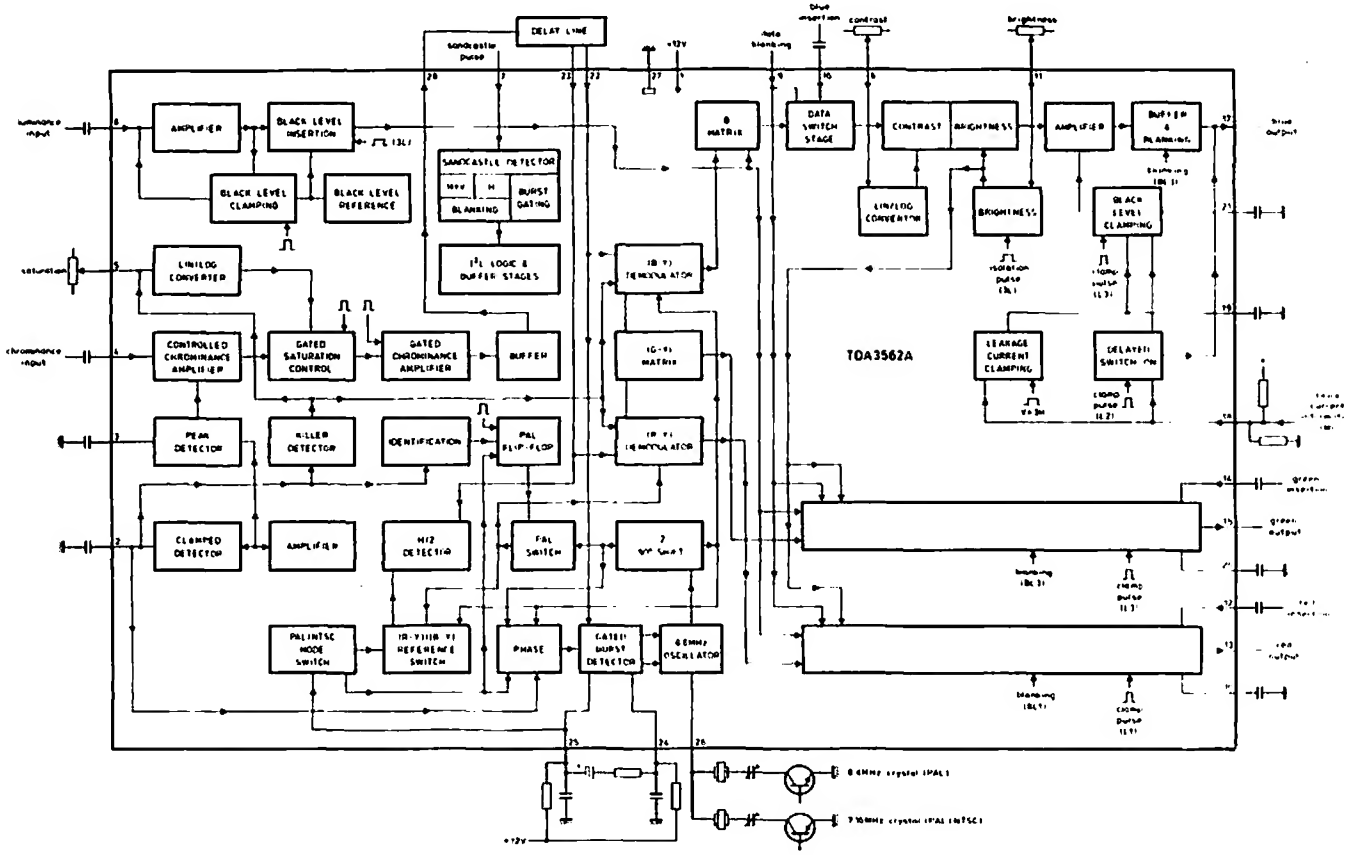

WF16
0.2V 10uS
H
2V
WF17
0.2V 10uS
H
3V

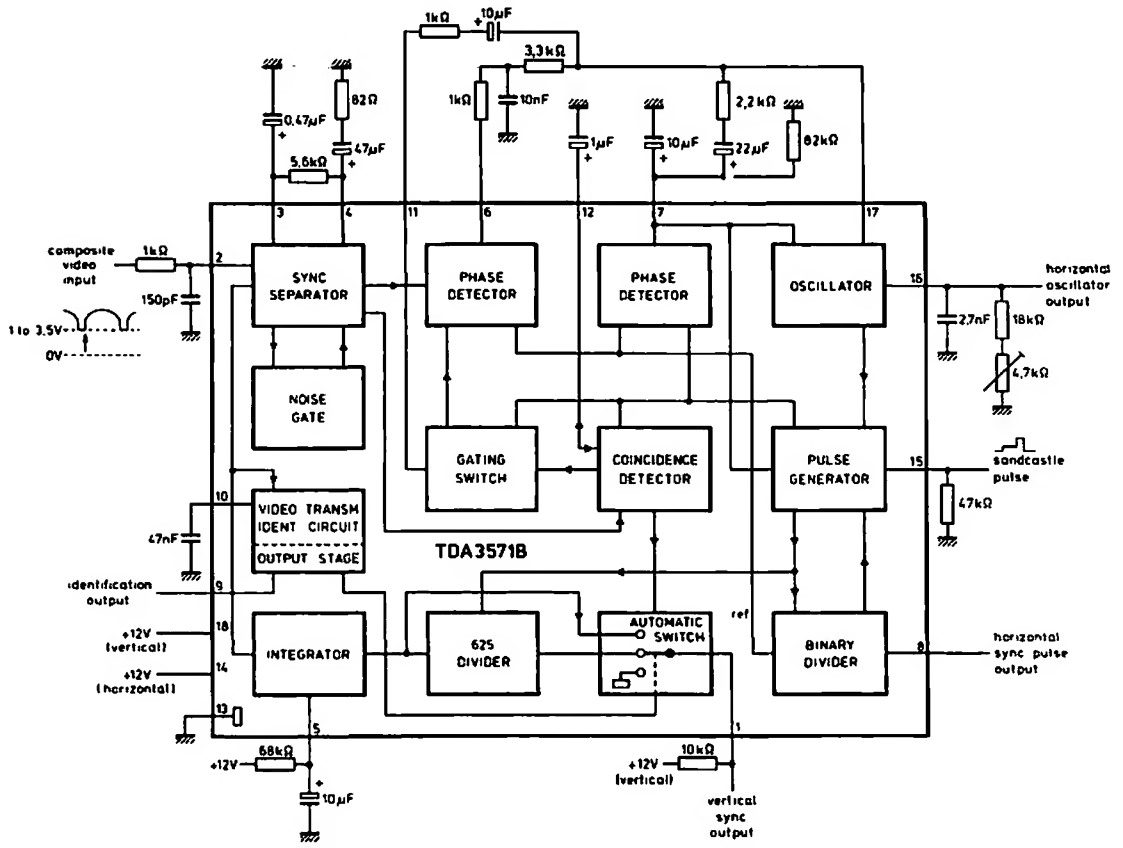

WF22
5V 10uS
0V
WF23
2V 10uS
6.2V
3.4V

MC 1377P ENCODER



TDA 3562A DECODER




1kΩ
10µF
3,3kΩ
1kΩ
10nF
1µF
10µF
2,2kΩ
22µF
82kΩ
0,47µF
82Ω
47µF
5,6kΩ
composite video input
1kΩ
150pF
1 to 3,5V
0V
SYNC SEPARATOR
PHASE DETECTOR
PHASE DETECTOR
OSCILLATOR
horizontal oscillator output
27nF
18kΩ
4,7kΩ
NOISE GATE
GATING SWITCH
COINCIDENCE DETECTOR
PULSE GENERATOR
sandcastle pulse
47kΩ
VIDEO TRANSM IDENT CIRCUIT
OUTPUT STAGE
47nF
TDA3571B
identification output
+12V (vertical)
+12V (horizontal)
INTEGRATOR
625 DIVIDER
AUTOMATIC SWITCH
ref
BINARY DIVIDER
horizontal sync pulse output
68kΩ
+12V
10µF
10kΩ
+12V (vertical)
vertical sync output

Introduction

The CVI-07P Chroma Board is designed to provide correct subcarrier and PAL phase locking for CVI-03 rev 4 and rev 4A PAL video boards. It bolts to the side of the video board and attaches to various points by way of six connectors and associated leads.

When the CVI is used in conjunction with a video mixer the chroma and PAL phase on the mixer video input is required to be stable. In this situation the installation of CVI-07P is recommended. In situations where chroma phase and PAL phase are not as important (e.g. a two VCR machine edit suite without mixing effects) there may be no obvious benefit gained from installing CVI-07P.

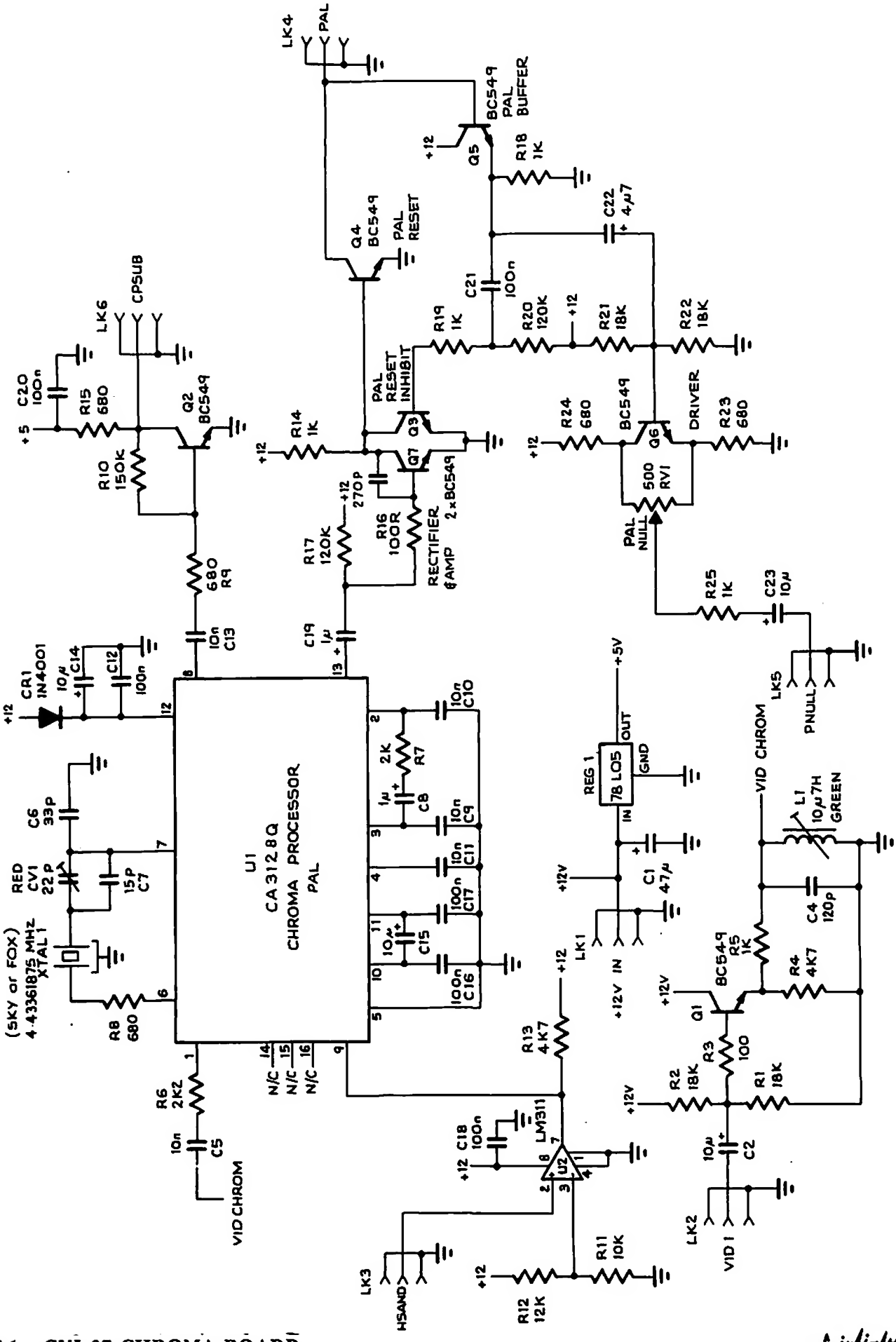
Circuit Description

The video signal via connector LK2 from the VIDEO 1 input is buffered by Q1 and filtered by L1 and C4 to provide a chrominance only signal to pin 1 of the chroma-processor U1. A burst gate signal is derived from the sandcastle signal via LK3 by comparator U2 and passed to U1. Using the burst gate and chroma signals the chroma-processor U1 locks a crystal oscillator formed by crystal XTAL1, CV1, C7, C6 to the subcarrier burst frequency. The free-running oscillator frequency is set by CV1. A 1vp-p continuous sinusoidal subcarrier signal is available at pin 8 of U1 and is squared up to TTL levels by Q2 and sent to the Video Board via LK6.

A PAL phase signal is available at pin 13 of U1. The negative going peaks of this signal are amplified by Q7 which provides a reset signal to Q4 if not inhibited by Q3. Q5 buffers the PAL phase signal via LK4 from the encoder IC on the video board. This is amplified by Q3 which inhibits the reset pulse from Q7 whenever the PAL phase from the encoder is high. This is the in-phase condition. If a reset pulse is generated by Q7 when the encoder PAL phase is low (the out-of-phase condition) then Q3 is off and the reset pulse turns on Q4 which pulls the encoder PAL signal via LK4 to 0v, causing the encoder to change the PAL phase. The reset pulse needs to be inhibited during the in-phase condition because the pulse occurs during the burst period and interferes with the normal functioning of the encoder burst generation. Thus resets only occur when the internal and external PAL phases do not match.

Buffer Q6 provides a bipolar PAL phase signal to the encoder R-Y clamp via LK5. The level of this signal can be adjusted accurately through zero by RV1 to allow subcarrier feedthrough nulling within the encoder.

The +12v supply via LK1 from the video board is smoothed by C1. The +11.3v for U1 is supplied by CR1 and smoothed by C12 and C14. The +5v rail is generated by REG1 from the +12v rail.


LK4
PAL
BC549
PAL
BUFFER
Q5
+12
R18
1K
C22
4.µ7
Q4
BC549
PAL
RESET
C21
100n
LK6
CPSUB
R19
1K
R20
120K
+12
R21
18K
R22
18K
C20
100n
+5
R15
680
Q2
BC549
PAL
RESET
INHIBIT
Q3
R14
1K
+12
Q7
+12
270P
R24
680
BC549
Q6
DRIVER
R23
680
+12
R10
150K
R16
100R
2xBC549
RECTIFIER
&AMP
R17
120K
500
RV1
PAL
NULL
680
R9
R25
1K
C23
10µ
10n
C13
C19
1µ
LK5
PNULL
CR1
IN4001
10µ
C14
C12
100n
+12
+5V
VID CHROM
REG 1
78 L05
OUT
GND
IN
L1
10µ7H
GREEN
U1
CA3128Q
CHROMA PROCESSOR
PAL
2K
R7
1µ
C8
10n
C10
10n
C9
10n
C11
100n
C17
10µ
C15
100n
C16
C6
33P
RED
CV1
22P
15P
C7
(SKY or FOX)
4.43361875 MHz
XTAL1
R8
680
+12V
C1
47µ
LK1
+12V IN
C4
120P
BC549
Q1
R5
1K
R4
4K7
+12V
R2
18K
R3
100
R1
18K
+12V
R6
2K2
10n
C5
VID CHROM
N/C
N/C
N/C
R13
4K7
+12
C18
100n
LM311
U2
10µ
C2
LK2
VID 1
LK3
HSAND
R11
10K
+12
R12
12K

Equipment Required

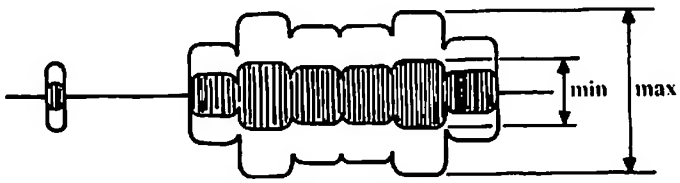
- CVI with calibrated CVI-03P rev 4 or rev 4A and modifications and connections for CVI-07P
- Oscilloscope, dual channel, 100MHz
- Vectorscope (PAL)
- Monitor (PAL composite or RGB)
- Test Signal (Colour Bar) Generator (PAL)
- Frequency Meter (upto 10MHz with 6 digit accuracy)

Setup

- Refer to the "General Test Setup" section in the CVI Service Manual for connecting test equipment.
- Connect CVI-07 to modified CVI-03.
- Connect PAL Colour Bars signal to VIDEO 1.
- CRO - sweep 100ns div.
  - CH-1 0.5V div, AC, on pin 1 of U1 (CA3128).
  - trigger AC on CH-1.
- Frequency meter - middle pin of LK6.
- Vectorscope - reference and sync CH-A, NTSC display, input CH-B.

Procedure

With colour bars input and observing CH-1 on the CRO, adjust the inductor L1 so that the chroma signal on pin 1 of U1 is set to a maximum. See following diagram. This sets the centre frequency of the chroma bandpass filter around the subcarrier frequency.



Chroma adjusted to be maximum

Subcarrier Frequency Adjustment

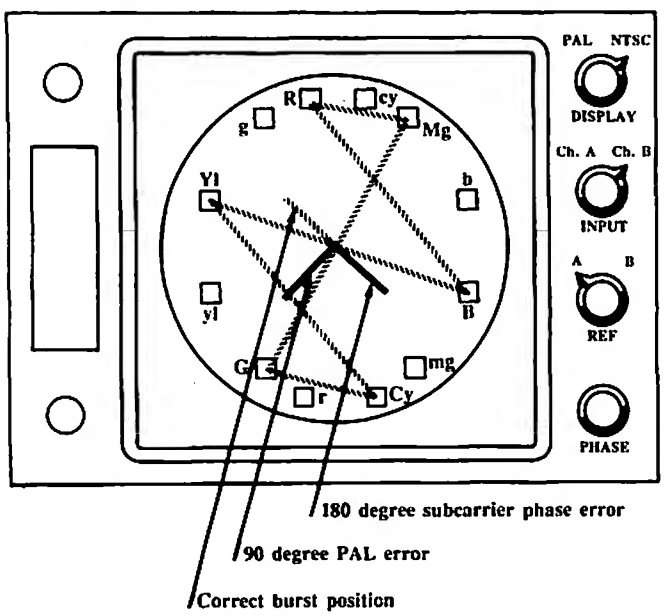
- Connect CH-1 to the middle pin of LK6.
- Disconnect the signal to VIDEO 1.
- The CH-1 signal should be a TTL square wave (low: <0.8v, high: >2.4v).
- Adjust CV1 so that the subcarrier frequency is 4.433619 MHz +-5Hz.
- Reconnect the video input to VIDEO 1 and check that the frequency is within the above limits.
- Disconnect the signal to VIDEO 1 again and check that the frequency is still within limits. This sets the free-running frequency of the internal subcarrier reference oscillator.

PAL and Subcarrier Phase
(Oscilloscope Method)

- Connect a video signal to VIDEO 1 input.
- Check that the CVI-07 locks to the incoming subcarrier on the vectorscope.
- Check the signal on the middle pin of LK4. This should be a 2Vp-p square wave at half line rate. When the signal to VIDEO 1 is disconnected and reconnected this PAL square wave should be pulled to ground for one or two lines during the burst period (reset pulses). These reset pulses should only occur when there is an interuption to the normal PAL pulse sequence (i.e. at the point when the input is connected or disconnected, glitch off tape signal etc.). No reset pulses should occur when there is no input to VIDEO 1.

PAL and Subcarrier Phase
(Vectorscope Method)

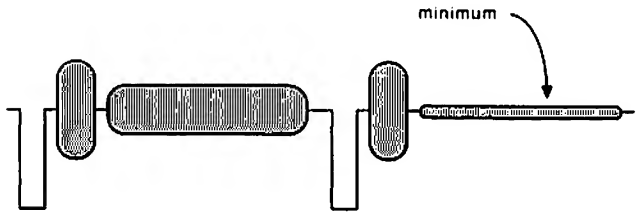
- Connect a PAL colour bar signal to VIDEO 1 input.
- Select CH-B and NTSC display on the vectorscope.
- Check that the CVI-07 locks to the incoming subcarrier on the vectorscope.
- Align the vectorscope and the CVI subcarrier phase so that the burst vectors overlap and are positioned over the top burst mark (see diagram below).



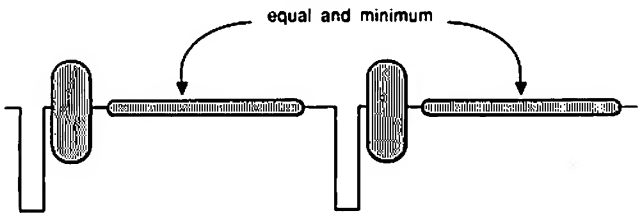
- Disconnect and reconnect the signal to VIDEO 1 several times. The vectorscope display should always revert back to the original display when the signal is reconnected indicating that subcarrier and PAL phase are being detected correctly from the incoming video.
- With an input to VIDEO 1 turn the CVI off and on several times and again check that the vectorscope display aligns correctly.

Procedure

a) Clear the screen to black using preset 3 with the value control set to zero.
b) Adjust RV14 and RV15 on CVI-03P to obtain minimum chroma in the picture area on a particular line. See diagram below.



c) Adjust RV1 on CVI-07P so that any chroma feedthrough on consecutive lines is equal. See diagram below.



d) Re-adjust RV14, RV15 on CVI-03P and RV1 on CVI-07P to obtain minimum chroma feedthrough in the picture area on consecutive lines.
e) Select preset 97 and check that the colour bar waveforms on consecutive lines are the same.

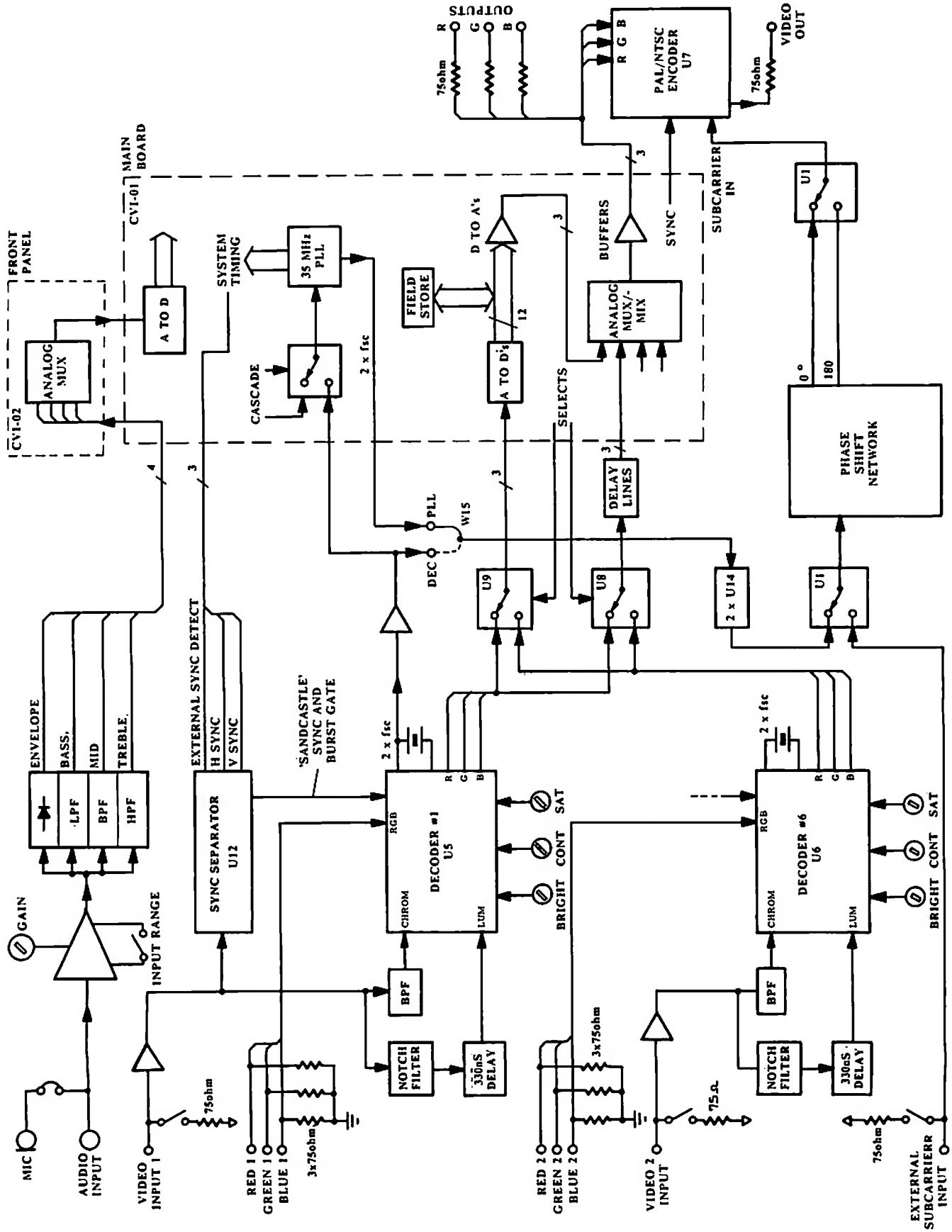
This test procedure checks that the CVI output PAL phase and subcarrier phase are locked to the incoming video signal on VIDEO 1 input. Several PAL reset pulses will be visible on pin 20 of encoder U7 for a short period after the signal to VIDEO 1 input is connected but should not appear at any other time unless there is a disturbance to the PAL sequence on the input signal.

Video Board - NTSC 4

CONTENTS

CVI-08 Sync separator

BLOCK DIAGRAM



1. **Audio input** is selected from either the internal microphone or an external source. The external source is selected when a plug is inserted into the audio input jack on the back panel. [CVI03-1]

2. **Audio amplifier** amplifies the selected input signal to levels required by the following filter and detector stages. The gain of the amplifier may be set to low or high using Switch 1 No.1 (SW1/1), and adjusted using the Audio Sensitivity control. [U13,U14, CVI03-5]

3. **Audio analyser** consists of three filters: lowpass (200Hz) for bass, bandpass (400-800Hz) for midrange, highpass (800Hz) for treble. The output of each filter drives an envelope detector, the output voltages of which represent the energy in that particular audio bandwidth. A fourth detector is used to detect the overall envelope. These four signals (0-3.2V) are passed to the analog multiplexer on the front panel and on to the ADC. [U14, CVI03-5]

4. **Sync separator** derives video timing signals from Video 1 input. The signals that U6 generates are:

External sync detect. When U12 determines that the external video is absent or poor quality then pin U6/10 goes high, causing the output of U7/7 to go high. With acceptable external video present U6/10 goes low, resulting in a low output from U7/7. This signal is used on the main board to select the appropriate timing signals. It is also used to turn on the FET Q12 when external video is absent. This prevents the PAL decoder U4 from trying to lock its crystal oscillator to any noise on the video input and stabilises the crystal running frequency.

Vertical sync. When acceptable external video is present U6/1 outputs positive going vertical sync pulses which are buffered by U12/5,6. When no external video is present these pulses are inhibited.

Sandcastle. (Horizontal Sync and Burst Gate) U12/15 produces a positive going, multilevel pulse. The lower level provides Hsync timing and the higher level provides burst gating. Comparator U8 detects H.sync from the sandcastle for the main board timing. A vertical blanking signal (SBLANK) from the main board is added to the sandcastle signal by R142 and D2. The resultant signal is used by the decoders U4 and U5.
IC U9 buffers the sandcastle signal to the decoders.

Internally the 2575 consists of:
a. A sync separator that samples the input video black level on U6/4, R120, C94 and generates a sync slicing level proportional to the input sync amplitude via R121, U6/3. A two times H frequency oscillator whose frequency is set by C125, R134, VR5 and the voltage on pin 15 and which is phase locked to the external video H via the RC networks on U6/7,9 and 6. The response time of the phase lock loop is made slow or fast (depending on whether the oscillator is locked or not) by clamping or open circuiting U6/9.

b. A vertical sync integrator and detector, U6/5, R127, C91.

c. A 625 line divider, coincidence detection and signal switch which is used to generate the vertical sync output in two different ways depending on the quality of the external video. The Vsync can be generated internally by the divider or taken from the external sync integrator.
For more detailed information refer to the Philips publication "Bipolar ICs for video equipment, 1983." [U6, TDA 2575], (CVI03-4)

5. **Video input buffers** consist of emitter followers Q13 and Q16 buffer the video 1 and 2 inputs. Their outputs drive the bandpass and notch filters for the two decoder ICs. Q13 (input 1) also provides the video signal to the sync separator U6. [CVI03-2 and 3]

6. **Notch filter** removes the colour subcarrier (3.58MHz) from the composite video signal. The remaining luminance information at the output is passed to the decoder via the 330nS delay lines. [L6,C51,L15,C79,C68], (CVI03-2 and 3)

7. **Bandpass filter** passes only the colour subcarrier component of the incoming video signal to the chrominance input of decoder. [L4,C49,L5,C77], (CVI03-2 and 3)

8. **330nS delay line** in the luminance signal path compensates for the delay of the chrominance signal through the bandpass filter and the decoder. This ensures that the two signals remain synchronised. [CVI03-2 and 3]

9. **Decoder 1** generates red, green and blue (RGB) signals from the composite video 1 input. Synchronisation is taken from the sync separator (4). The decoder output is either the direct RGB signals from RGB input 1 or the RGB signals decoded from composite input 1, depending on the position of SW1/8.

The crystal on U4/26 runs at twice the colour subcarrier frequency. It locks to the external video subcarrier if present or free runs if no video is present. The signal from the crystal is also passed to the subcarrier amplifier for use by the digital board and the encoder. To prevent noise on video 1 input line affecting the operation of the crystal oscillator when no external video is present, the FET Q12 is used to short U4 pins 24 and 25 together. This disables the gated burst phase detector that controls the crystal oscillator.

The 'Hue' trimpot VR8 controls the phase of the reference drive to the burst phase detector in the TDA 3562 by varying the voltage at pins 24 and 25 between 7.5V and 8.5V. The RGB outputs from the TDA 3562 are intended to drive the RGB gun drive transistors of a TV set and so have an automatic "black level" control input pin U4/18.

Resistors R68,R69,R70 and R71 are used to maintain the RGB outputs at the correct DC level. The colour saturation control pin U4/5 is bidirectional. When colour video is present it is an input controlled by the SAT. pot VR11, and can be forced low to kill colour by jumper LK4. When there is insufficient colour burst on the external video the TDA 3562's colour killer circuit pulls pin 5 low, but it may be forced high by jumper W1 to "unkill" colour.

The output (U4/28) to the phase splitter Q10 contains chrominance informance only. The complementary signals from Q10 are passed via pins 22 and 23 to the chrominance demodulators in the TDA 3562. Q11 provides a constant current sink on the Q10's emitter. In the signal on pin 28, the burst is at a constant level and the level of the picture chrominance is variable, controlled by the saturation input pin U5/5, and the kill/unkill jumper LK4.

10. **Decoder 2** generates red, green and blue (RGB) signals from the composite video 2 input. Synchronisation is taken from the sync separator (4). The decoder output is either the direct RGB signals from RGB input 2 or the RGB signals decoded from composite input 2, depending on the position of SW1/7. [U5, TDA 3562], (CVI03-3)

11. **Picture controls** Decoders 1 and 2 have separate brightness, contrast and saturation control pots, which vary the control voltages to pins 11,6 and 5 of the decoders. If direct RGB inputs are selected to the decoders only the

brightness and contrast controls will affect the decoder outputs. [CVI03-2 and 3]

12. **Video source multiplexers** select the inputs to the digital and analog paths through the CVI. Each path may take its input from the RGB outputs of either Decoder 1 or Decoder 2. The selection is made using two control lines from the digital card, ASEL1 and ASEL2. These TTL signals are buffered to 12V levels by open collector gates U12/1 and 3. When ASEL1 and 2 are low decoder #1 RGB outputs are selected, and when high Decoder #2 outputs are selected. [U10,U11, CVI03-4]

13. **660nS delay lines** at the start of the analog path compensate for the delays caused by digitising and processing on the digital path. The delay ensures that picture information sent through the two paths retains horizontal registration. [L7,8,9,10,11,12], (CVI03-4)

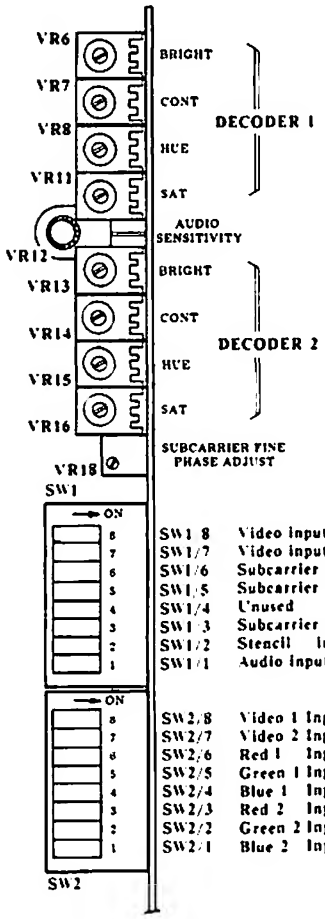
14. **Frequency divider** halves the frequency of the twice-subcarrier signal from the phase-locked loop or Decoder 1. Its output provides the internal subcarrier reference to the phase shifter for use by the encoder. [U1, CVI03-1]

15. **Subcarrier phase shifter** takes its input from either the External input or the frequency divider, depending on the position of SW1/6, which provides the SUBSEL signal to U15. SW1/5 provides a coarse phase shift of 0 or 180 degrees by selecting the Q or NOT Q outputs of U16/5,12. The subcarrier trimmer VR5 allows fine adjustment by varying the pulse width from the other half of U16. Together these give a full 360 degree range. Transistors Q4, Q25 and filter L2, C122 and C120 convert the rectangular output of the phase shifter to a constant level sine wave. This is passed to the encoder subcarrier input via VR17 which sets the correct level required by the encoder IC. [U15,U16], (CVI03-5)

16. **Encoder** generates a full composite PAL colour signal from RGB, composite sync and subcarrier inputs. The output (pin 9) can directly drive a 75-ohm cable. The RGB inputs are capacitively coupled. Clamping is done on various signals in the MC1377 using external capacitors C7, C8, C9 and C10. Trimpots VR2 and VR3 vary the bias current to the R-Y and B-Y clamp pins and are used to null the amount of residual colour carrier in black. VR4 varies the bias to pin 19 which alters the phase of the R-Y modulator. These adjustments require the use of a vectorscope. The MC1377 contains a ramp generator running at horizontal line rate, which is used to set the burst position in the output video. The slope of the ramp (and the burst position) is determined by VR1, R20 and C12 connected to U2/1. U2/16 is an 8.2V reference output voltage used as a stable source for the ramp generator. The bandwidth of the chroma signal generated by the MC1377 is limited by the bandpass circuit (C13, L1, C130) between U2 pins 13 and 10. This delays the chroma by about 350ns and so the luminance must also be delayed by the same amount. This delay is provided by L2 between pins 6 and 8 of U2.

The composite sync signal to U7/2 is derived from the digital board. The subcarrier input U7/17 comes via the phase shifter from either external or internal sources.

For more information, refer to Motorola's "Application of the MC1377 Colour Encoder". [U2 MC1377], (CVI03-1)

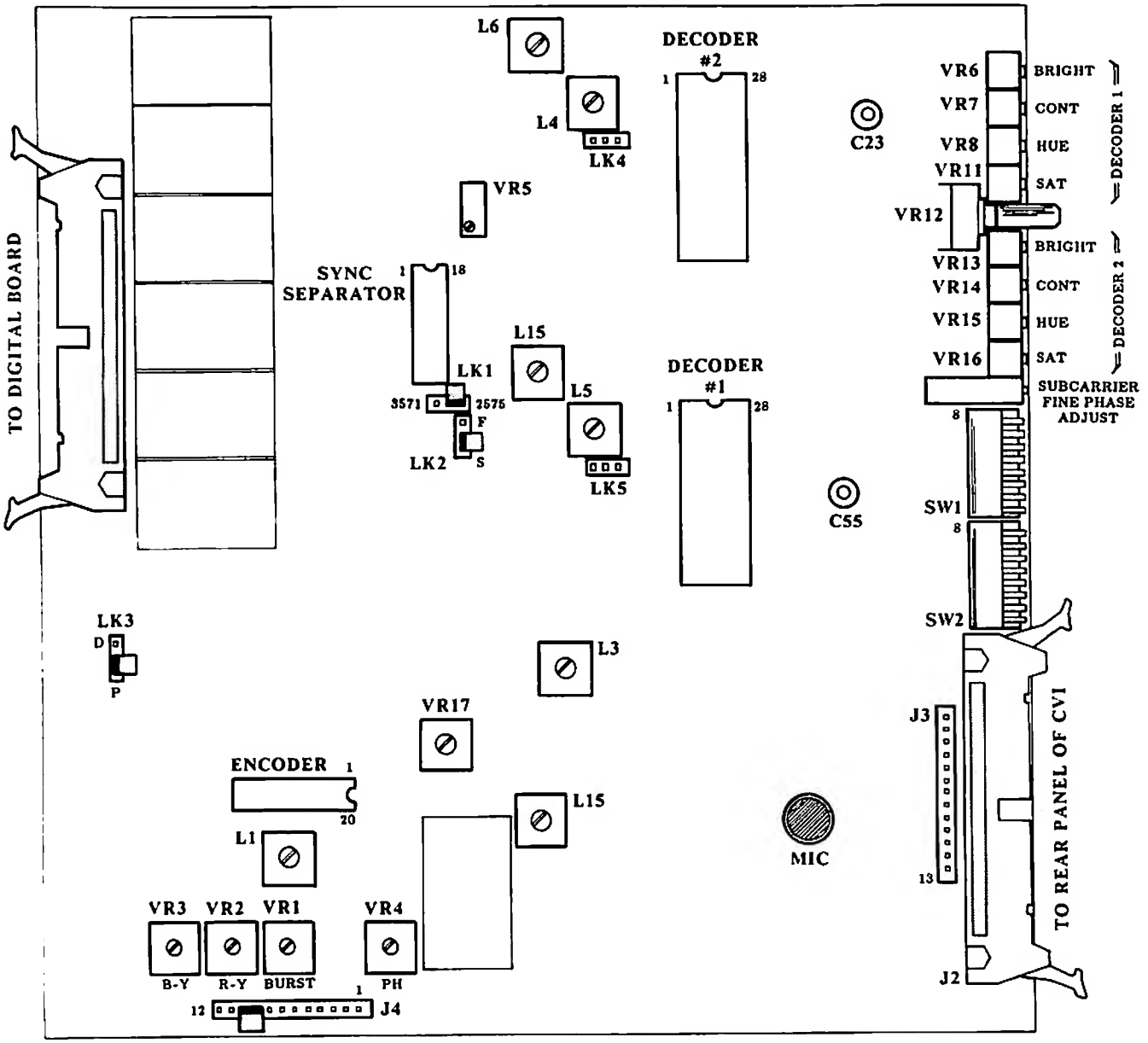


		OFF	ON
SW1/8	Video input 1 source composite	RGB 1	Video 1
SW1/7	Video input 1 source composite	RGB 2	Video 2
SW1/6	Subcarrier source	Ext subc I/P	Internal (1)
SW1/5	Subcarrier phase coarse adj.	0 Degrees	180 deg (2)
SW1/4	Unused	-	
SW1/3	Subcarrier input terminate	-	75 ohms
SW1/2	Stencil input terminate	-	75 ohms
SW1/1	Audio input level range	Low	High
SW2/8	Video 1 Input terminate	-	75 ohms
SW2/7	Video 2 Input terminate	-	75 ohms
SW2/6	Red 1 Input terminate	-	75 ohms
SW2/5	Green 1 Input terminate	-	75 ohms
SW2/4	Blue 1 Input terminate	-	75 ohms
SW2/3	Red 2 Input terminate	-	75 ohms
SW2/2	Green 2 Input terminate	-	75 ohms
SW2/1	Blue 2 Input terminate	-	75 ohms

Notes

(1) The internal subcarrier is frequency (but not phase) locked to the VIDEO 1 input if video is present on it.

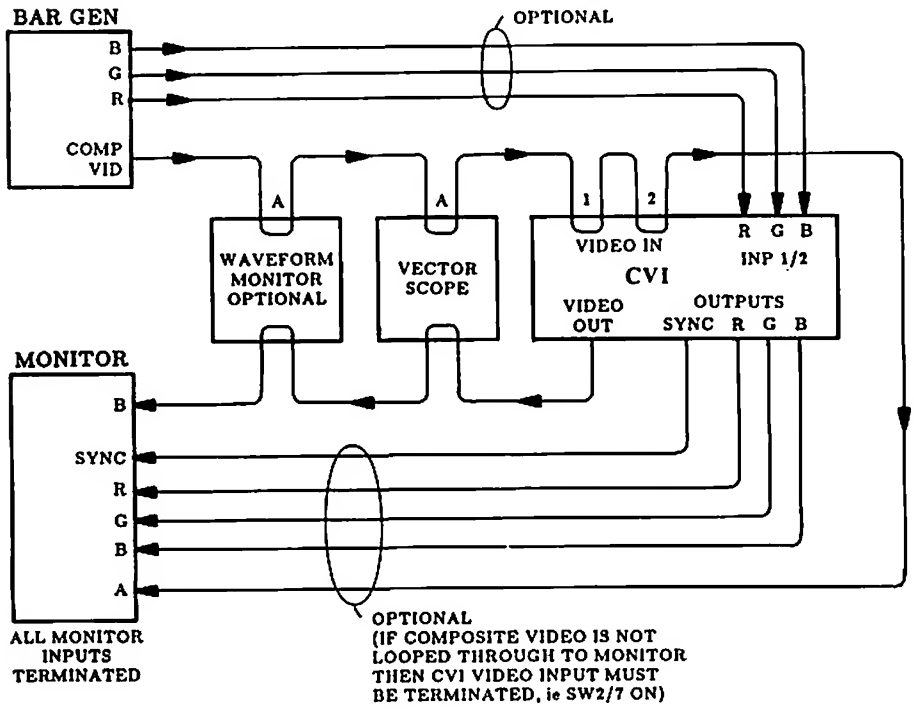
(2) SW1/5 selects a phase shift of zero or 180 degrees. Using it and the phase fine adjustment trimpot, the video output subcarrier phase may be adjusted from 0 degrees to 360 degrees relative to the reference subcarrier.

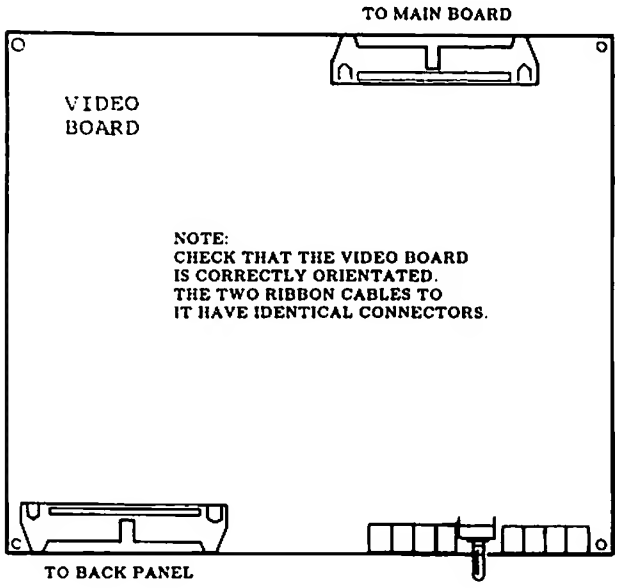

TO DIGITAL BOARD
L6
L4
LK4
VR5
SYNC SEPARATOR
1
18
LK1
3571
2575
F
S
LK2
L15
L5
LK5
DECODER #2
1
28
DECODER #1
1
28
C23
C55
VR6
VR7
VR8
VR11
VR12
VR13
VR14
VR15
VR16
BRIGHT
CONT
HUE
SAT
BRIGHT
CONT
HUE
SAT
DECODER 1
DECODER 2
SUBCARRIER FINE PHASE ADJUST
8
SW1
8
SW2
LK3
D
P
L3
VR17
ENCODER
1
20
L1
L15
VR3
VR2
VR1
VR4
B-Y
R-Y
BURST
1
PH
12
J4
MIC
J3
13
J2
TO REAR PANEL OF CV1

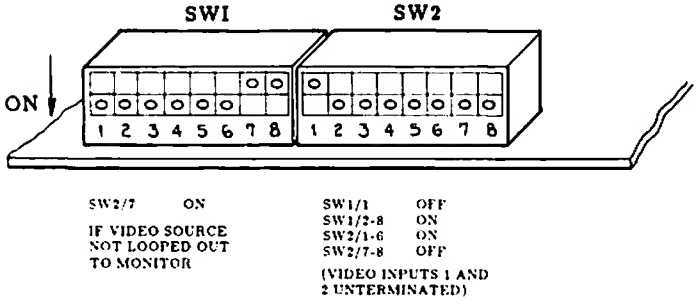
EQUIPMENT REQUIRED

a) 100MHz dual channel oscilloscope.
b) 6 to 7 digit 100MHz frequency meter.
c) NTSC Vectorscope.
d) NTSC 100% colour bar generator.
e) NTSC composite video monitor with RGB inputs.
f) NTSC waveform monitor (optional).
g) CVI system (main board, front panel, cables, etc.)

GENERAL TEST SETUP AND PROCEDURE







The diagram above shows original settings of SW1 and SW2

Jumper link settings (NTSC)

LK1 - 2575
LK2 - S
LK3 - D
Link J4 - Pins 9 and 10

General procedure

Due to the interactions between adjustments on the board, the following sequence of operations is recommended:

1) check and adjust sync separator
2) check operation of subcarrier amplifier
3) set free run frequency of subcarrier crystal
4) check that main board PLL locks to subcarrier
5) check and adjust subcarrier phase shift chain
6) check and adjust video encoder
7) check and adjust decoder #1
8) check and adjust decoder #2
9) check RGB inputs and outputs
10) check audio input

PRESETS USED IN SEVICING

The CVI PRESETS allow the internal state of the CVI to be quickly restored to a predefined condition. For a full description refer to the operation manual.
Only a few of the 100 presets available need to be used while servicing the videoboard. They are:

- 00 Selected at power on, displays the Fairlight logo
- 95 Video 2 through
- 96 Video 1 through
- 97 Internal colour bars

The preset number currently selected is displayed on the front panel LED display. To change the preset number, press the PRESET key followed by two number keys.

For example, **PRESET 9 5** for preset 95.

If the CVI has been in use it is possible that these presets have been changed by the user. In this case reset the above presets. Refer to the "RESET PRESETS" section of the user manual.

The effects and uses of these presets are as follows:

00 At power on, the Fairlight logo is drawn (in colour) in the CVI video RAM and stencil. If video is present on the Video 1 input the CVI locks to it. The Video 1 image is converted to analog RGB by decoder 1, then passed via mux U9 to the analog path on the main board. Simultaneously, the image in the RAM is read out and converted to analog RGB. The RAM image (the logo) and the incoming video are combined by the analog video MUX/MIX and then passed through buffers to the CVI RGB outputs and composite video encoder.
This preset is used while testing the sync separator, main subcarrier oscillator, subcarrier amplifier, MUX U9 and the phase shifter circuit.

95 Video input 2 through. The CVI locks to Video 1 input, and passes the Video 2 input through the analog path, i.e. decoder #2, MUX U8, delay lines, main MUX/MIX/buffers, RGB outputs and encoder.
This preset is used to test decoder #2.

96 Video input 1 through. The same as 95, but uses decoder #1.
This preset is used to test decoder #1.

97 Internal colour bars. The CVI locks to Video 1 input if present, but uses the RAM as the sole colour source. The processor writes a "colour bars" image to the RAM. The video route is - RAM, D to A's, MUX/MIX, buffers, encoder.
This preset is used to test and align the encoder.

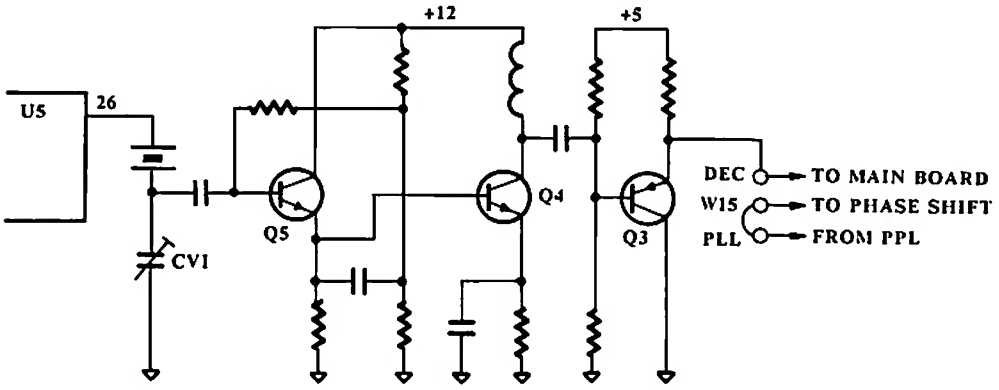
CONTENTS

NOTE: TTL levels implies a high (or 1) to be above 2.5V and a low (or 0) to be below 0.8V

Subcarrier amplifier

The crystal oscillator of the video 1 input decoder is used as the master frequency reference 2Fsc and locks to the video input subcarrier if video is present, or free runs if video is absent.

Transistors Q7, Q8 and Q9 amplify the low level signal from the crystal to TTL compatible levels.



Check the waveform at the D pin of LK3 for correct TTL levels, both with video applied to Video 1 input and with Video 1 disconnected.

Subcarrier crystal free run frequency

Setup

Connect the frequency meter to the D pin of LK3. Disconnect Video 1 and Video 2 inputs. Terminate Video 1 and Video 2 inputs (SW2/7, SW2/8). Adjust trimcap C23 for a frequency of 7.159090 MHz.

Subcarrier locking

Setup

- Link LK3 to "P".
- CRO - sweep 100nS/div.
- CRO - CH1 2V/div. on D pin of LK3.
- CRO - CH2 2V/div. on U1/9 (2Fsc divided by 2)
- CRO - trigger on CH1.
- Colour bars to Video 1 input.

The signal on CH2 should be a TTL square wave at 1/2 the frequency of CH1, and in steady phase lock.

Subcarrier phase shifter

This circuit is used to adjust the phase of the output video subcarrier relative to the input video subcarrier. A full 360 degrees range is possible using the coarse adjust switch and fine adjust trimmer.

The subcarrier source is selected (via U15) from either the external subcarrier input, or the Video 1 input decoder divided by two. Dual monostables U16 and trimpot VR18 provide the fine phase adjustment. One of the two outputs from U16 (0 or 180 degrees) is selected by U15 and SW1/5 and passed via the subcarrier filter L2 and level control VR17 to the encoder.

Setup

CRO

- Sweep 100ns/div
- Trigger on CH1
- CH1 1V/div, on U15/14 (4053, selected subcarrier)
- CH2 1v/div, on U2/17 (subcarrier input to encoder)

Procedure

To test the external subcarrier input amplifier, connect subcarrier to the input and check that the signal appears on CH1 when SW1/6 is off.

With SW1/6 on, set VR17 to midrange and adjust L2 for maximum amplitude and cleanest waveform at U7/17 (CH2). Next adjust the level pot VR12 for 0.75Vp-p at U2/17. The allowed range is 0.5Vp-p to 1Vp-p.

Check that SW1/5 moves the phase of U2/17 (CH2) by 180 degrees relative to U5/14 (CH1), and that VR18 also varies the phase.

Alternatively, if the rest of the board is working, supply colour bars to input 1, synchronise the vectorscope to the bar generator, select Preset 97 and view the CVI output on the vectorscope. Check that the CVI output burst can be rotated through 360 degrees using the coarse and fine phase controls.

Note: The division by two of the 2 x Fsc crystal oscillator on decoder 1 introduces a 0/180 degree ambiguity to the output subcarrier relative to the input subcarrier. Hence full colour lock cannot be guaranteed.

RGB, sync and stencil outputs

The RGB lines come directly from the main board, while the SYNC and STENCIL signals are generated on the main board and buffered by Q1 and Q2 on the video board.

Check these before proceeding to the encoder.

Setup

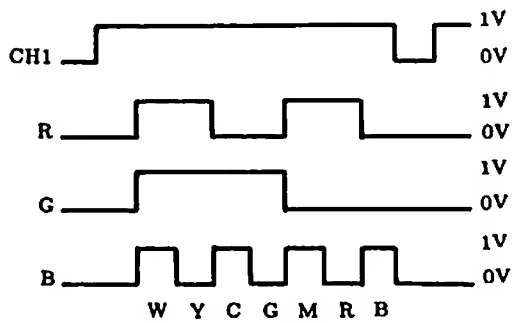
- Select preset 97 (internal colour bars)
- If your monitor has RGB inputs, connect the CVI's RGB and SYNC outputs to the monitor.

Check for a clean and correct colour bars image.

Otherwise -

- CRO - Sweep 10uS/division.
- CRO - CH1 0.5V/division. On SYNC OUT signal (with 75 ohm termination).
- CRO - CH2 0.5V/division. On R/G/B signal out (with 75 ohm terminations).
- CRO - Trigger on CH1, TV H sync.

Check for signals as indicated below:



Turn the CVI OFF. Wait for 5 or more seconds and turn ON, to obtain the startup logo.

Check that the STENCIL output is 1V p-p into 75 ohms. The signal will not be regular or coherent.

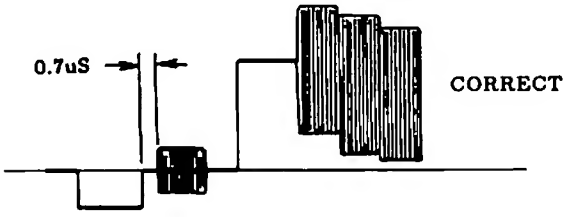
Video encoder

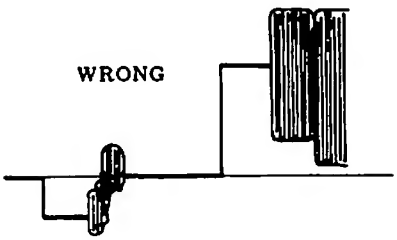
The NTSC encoder IC U2 takes RGB, subcarrier and sync inputs and generates composite colour video. Refer to page 4.14 for MC1377 block diagram.

Setup

- Preset 97 (internal colour bars).
- Select the CVI composite video output on the monitor, vectorscope and waveform monitor or CRO.

Adjust VR1 for correct colour burst position on the front porch as indicated below.

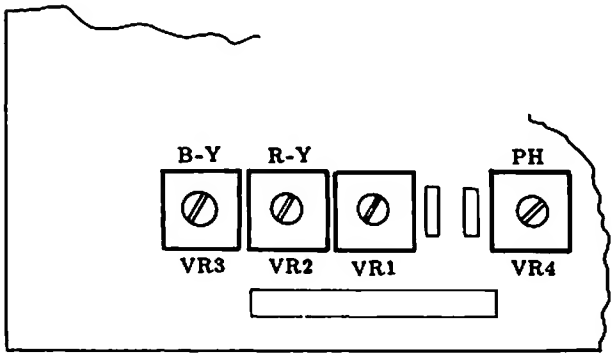




Adjust L1 for the straightest possible lines between colour points on the vectorscope.

Adjust VR4 pot for symmetrical vector display (U2/19).

Adjust VR2 (U2/12) and VR3 (U2/11) pots for minimum chroma on sync and front and back porches. Alternatively adjust these pots so that the central point of the vector display is centred on the grid.



Check the colour bars on the monitor for correct colour and hue.

Decoder #1 and #2 - TDA 3562

The NTSC decoder IC's U4 and U5 convert composite colour video to analog RGB signals. They require a multilevel "sandcastle" sync input signal for burst sampling, H syncs, etc. The external RGB inputs are processed and switched by the decoders also

Refer to the TDA 3562A block diagram on page 4.14

General Decoder Setup

View CVI RGB outputs on monitor. Alternatively, view CVI composite video out.

- 100% Colour bars to input 1 and 2.
- Brightness to minimum, saturation to mid range, contrast to maximum on both decoders.
- CRO - Sweep 10uS/division.
- CRO - CH1 0.5V/division on Video 1 input.
- CRO - Trigger on CH1, TV horizontal.

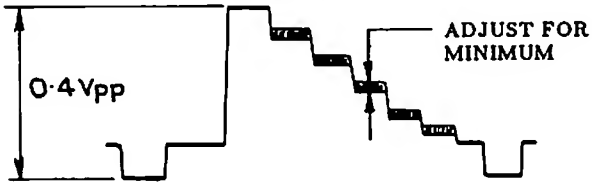
Decoder #1 setup

- Preset 96 (video 1 through).
- Set VR8 (HUE) to midrange.
- CRO - CH2 0.5V/division

The crystal oscillator free run frequency should have been set previously. See SUBCARRIER FREQUENCY section if frequency needs to be reset.

Connect CH2 to U5/4. Adjust L4 for maximum chroma amplitude.

Connect CH2 to U5/8. Adjust L4 for minimum chroma on the luminance signal.

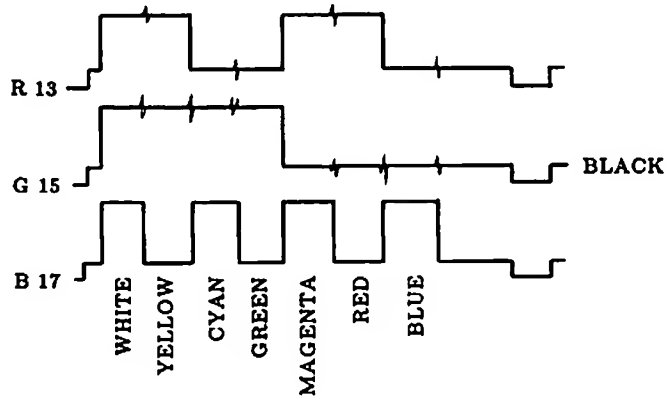


Setup

CRO - CH2 2V/division. On U4 pins 13,15,17 alternatively.

Adjust VR6 for correct hue, waveforms similar to below.

i.e., U4 pin



The aim is to get the tops and black levels of each waveform all lined up (equal levels).

Brightness and saturation controls also affect these waveforms.

Decoder #2 setup
- Preset 95 (video 2 through).
- Set VR15 (HUE) to mid range.
- CRO - CH2 0.5V/division.

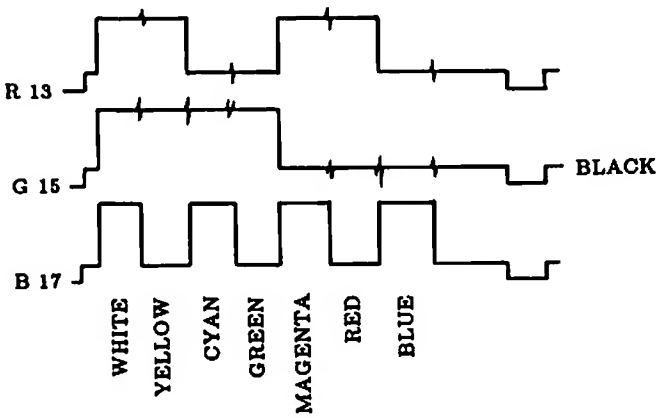
Adjust CV55 to the middle of the range in which colour appears on the screen. Remove video input 2, then put it back, checking that colour reappears when it is replaced. If not, readjust CV55.

Connect CH2 to U5/4. Adjust L5 for maximum chroma amplitude.

Connect CH2 to U5/8. Adjust L15 for minimum chroma on the luminance signal.

Setup
CRO - CH2 2V/division. On U6 pins 13,15,17 alternatively.
Adjust VR8 for correct hue.

i.e., U5 pin



The aim is to get the tops and black levels of each waveform all lined up (equal levels).

Several iterations may be required to get the best results.

RGB inputs

These are analog RGB inputs to the decoder chips U4 and U5. SW1/8 and SW1/7 select either RGB or composite on decoder #1 (U4) and decoder #2 (U5) respectively. See VIDEO CARD OPERATING CONTROLS.

To check RGB 1 inputs -

View CVI composite or RGB video output on monitor.
Select preset 96 (Video 1 through).
Apply colour bars to video 1 input.
Turn SW1/8 OFF. The colour bar output from the CVI should disappear (become black).
If the bar generator has RGB outputs, connect them to the CVI RGB 1 inputs and check for correct bars output from the CVI. Otherwise, loop the composite video bars signal through to the RGB 1 inputs one at a time and check for R,G and B images out of the CVI. Note that there should be only one termination on the video input, so either the RGB inputs or the video input should be unterminated.

To check RGB 2 inputs -

Select preset 95. (Video 2 through)
Apply colour bars to Video 1 and loop through to Video 2.
(Only terminate Video 2.)
Turn video board switch 1/7 OFF. The colour bar output from the CVI should disappear (become black).
Apply RGB bars or composite video to the RGB 2 inputs while observing the CVI output as for the decoder #1 procedure above.

Audio input

The audio input circuit consists of op amp U13 with a high or low gain selected by SW1/1, followed by the sensitivity pot VR12. The internal microphone or an external line level input are selected automatically by the external input socket. The signal is passed to a peak detector, a low pass filter, a band pass filter and a high pass filter, giving Envelope, Bass, Mid and Treble signals. These are sent to the multiplexer on the front panel to be digitised.

The audio analyser can be tested either by observation on a CRO, or by use of the CVI Testing ROM software (see your distributor).

Setup

- Set the audio sensitivity pot VR12 to 3/4 (clockwise).
- Set SW1/1 ON.

Quick check

Using either an external microphone plugged into the AUDIO INPUT jack on the back of the CVI, or the internal microphone MIC1 on the video board, check that sounds picked up by the microphone affect the voltage levels at the test points on the video board.

Connect a line level (200mV pp or greater) music source to the external input jack. Adjust the audio sensitivity pot VR12 for optimum response.

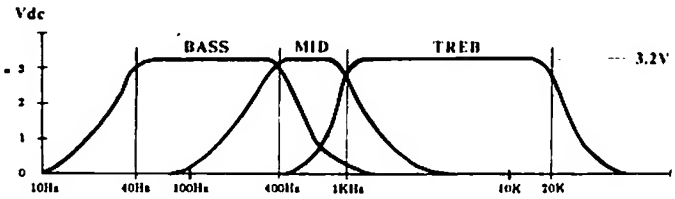
Detailed check

Equipment required

Audio oscillator
DC voltmeter
Oscilloscope

Setup

- Disconnect the back plane to video board ribbon cable from P1 on the video board.
- Connect the audio oscillator sine wave output to the video card AUD input at P2/7 and adjust the level to 1V pp (keep constant for all measurements).
- Set SW/1 on.
- Adjust the SENS pot VR12 for 7V pp at U14/1 (just less than the level at which the signal clips on the positive peaks) with a 1kHz input signal.
- While varying the input frequency and observing the DC voltages at the BASS, MID and TREB test points, check that the filter characteristics are approximately as follows.



Operating adjustments

These consist of the ten pots and sixteen switches on the edge of the video board.

To adjust the video control pots -

Select Presets 96 and 95 alternately.
Connect colour bars to Video inputs 1 and 2.
View the output of the CVI on the monitor
Flip between Presets 96/95 (external video) and Preset 97 (internal bars).
Adjust the Brightness, Contrast, Hue and Saturation controls so that the CVI internal colour values (Preset 97) match the external video range (Preset 96/95). For example, the two white values should be equally bright, etc. This may have to adjusted for various source material.

The video/RGB/stencil and subcarrier termination switches should be set ON for the signal cables that terminate at the CVI, and OFF for those that are looped through the CVI.

The fine phase adjust and audio sensitivity pots are set depending on the installation.

Notes 1. The tests for each section should be carried out in the CVI Preset indicated.

2. The components to be adjusted in each test are indicated in square brackets.

TEST	TEST POINT	EQUIPMENT
SETUP Set DIP switches. Set jumper links.		
SYNC (Preset 00) Check against video input: - sandcastle position and levels [VR10] - EXTSYNC signal - horizontal sync signal - vertical sync signal	 U4/7 U7/7 U8/7 U12/6	
SUBCARRIER (Preset 00) Check: - Subcarrier amplifier output > 2.5V - Subcar. oscillator free run frequency NTSC 7.159090 MHz [C23] - PLL lock - External subcarrier input amp. [SW1/6] - Subcarrier filter [VR17,L2] - Subcarrier level [VR17] - Subcarrier phase shift [SW1/5,VR18]	 LK3 (D) LK3 (D) LK3 (D) Vs U1/9 U15/4 U2/17 U2/17	 Vectorscope
RGB OUTPUTS AND STENCIL (Preset 00) Check.		CRO or RGB Monitor
ENCODER (Preset 97) Adjust: - Burst position [VR1] - Chroma filter [L1] - Chroma balance [VR2,VR3,VR4]		 CRO Vectorscope Vectorscope
DECODER 1 (Preset 96) Adjust: - Maximum chroma [L4] - Minimum chroma [L6] - NTSC Hue [VR8]	 U4/4 U4/8 U4/13,15,17	 Monitor
DECODER 2 (Preset 95) Adjust: - Maximum chroma [L5] - Minimum chroma [L15] - NTSC Hue [VR8]	 U5/4 U5/8 U6/13,15,17	 Monitor
RGB INPUTS 1 & 2 (Presets 96 & 95) Check.		 Monitor
AUDIO INPUT Check. [SW2/1,VR12]		 Monitor
COLOUR LEVELS (Presets 95,96 and 97) Adjust: [VR6,VR7,VR11,VR13,VR14,VR16]		 Monitor

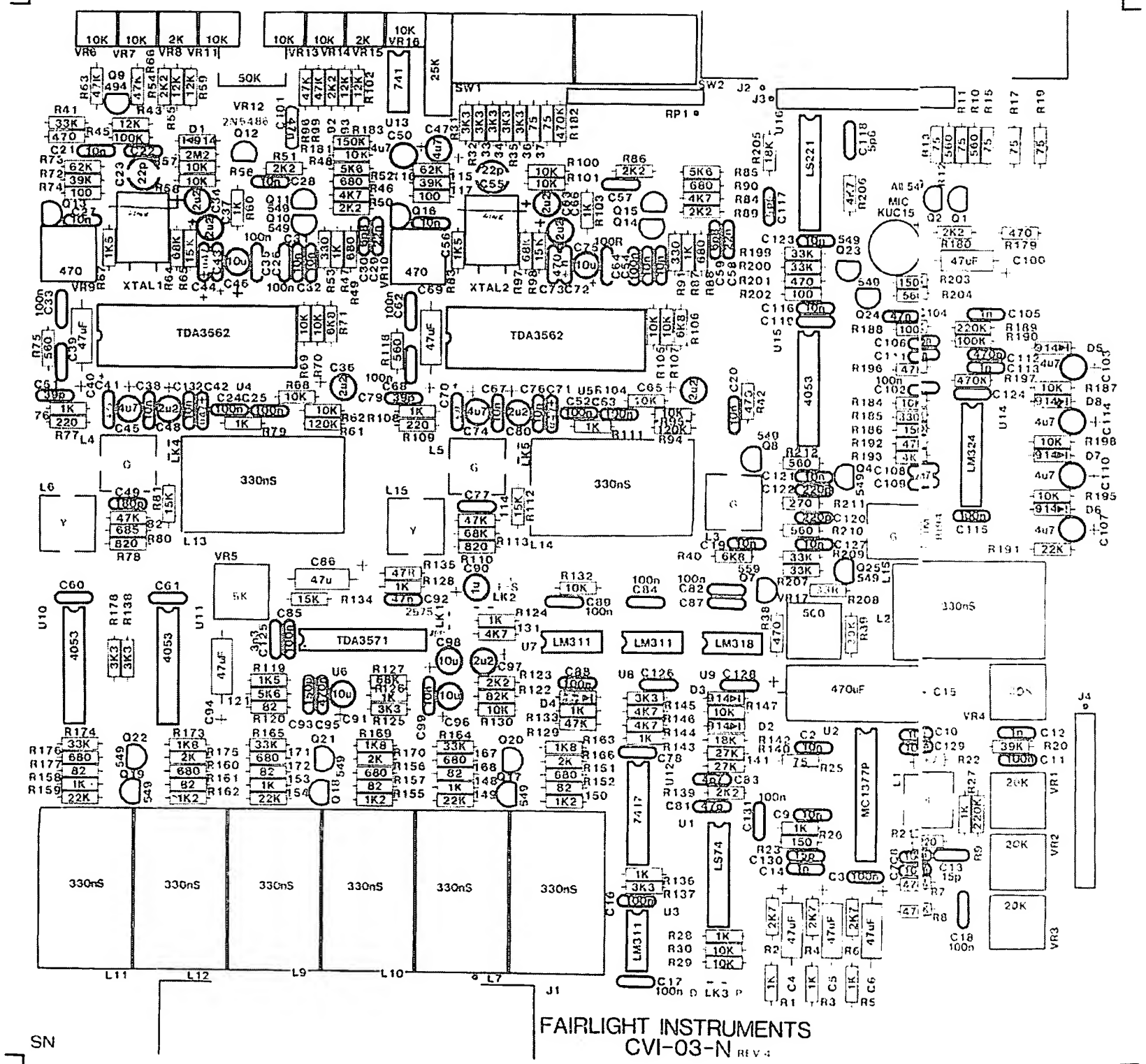
FAULTS & POSSIBLE CAUSES

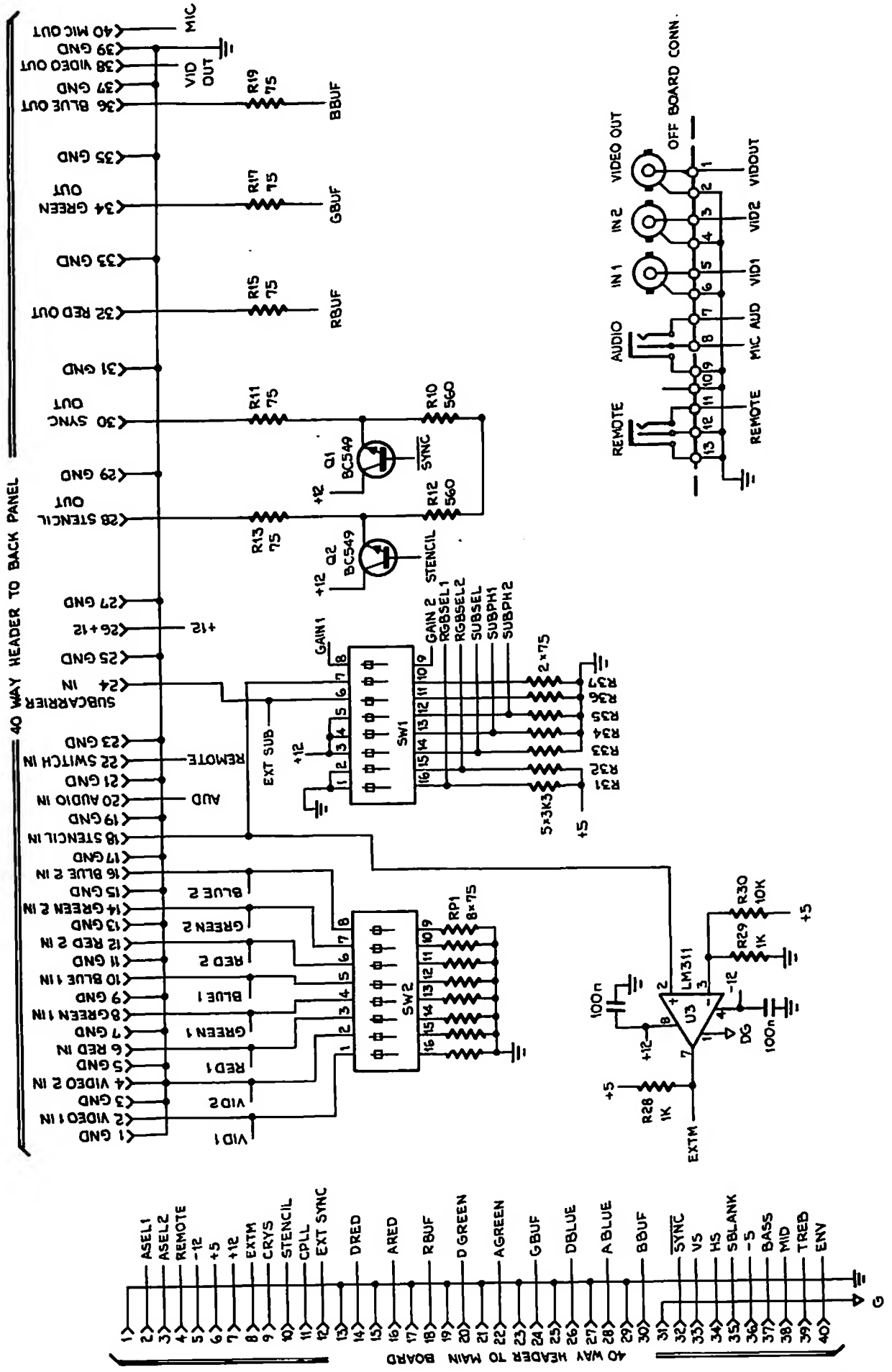
1) Loss of colour on output in internal sync mode (no external video).
- Decoder #1 XTAL OSC free run frequency wrong (not 2 x Fsc)
- Move LK3 to D position. If colour returns then main board PLL is not locking to video subcarrier.
- Divider U1 or phase shift chain faulty. Check that the modulator is getting subcarrier.
- Burst is in the wrong position.

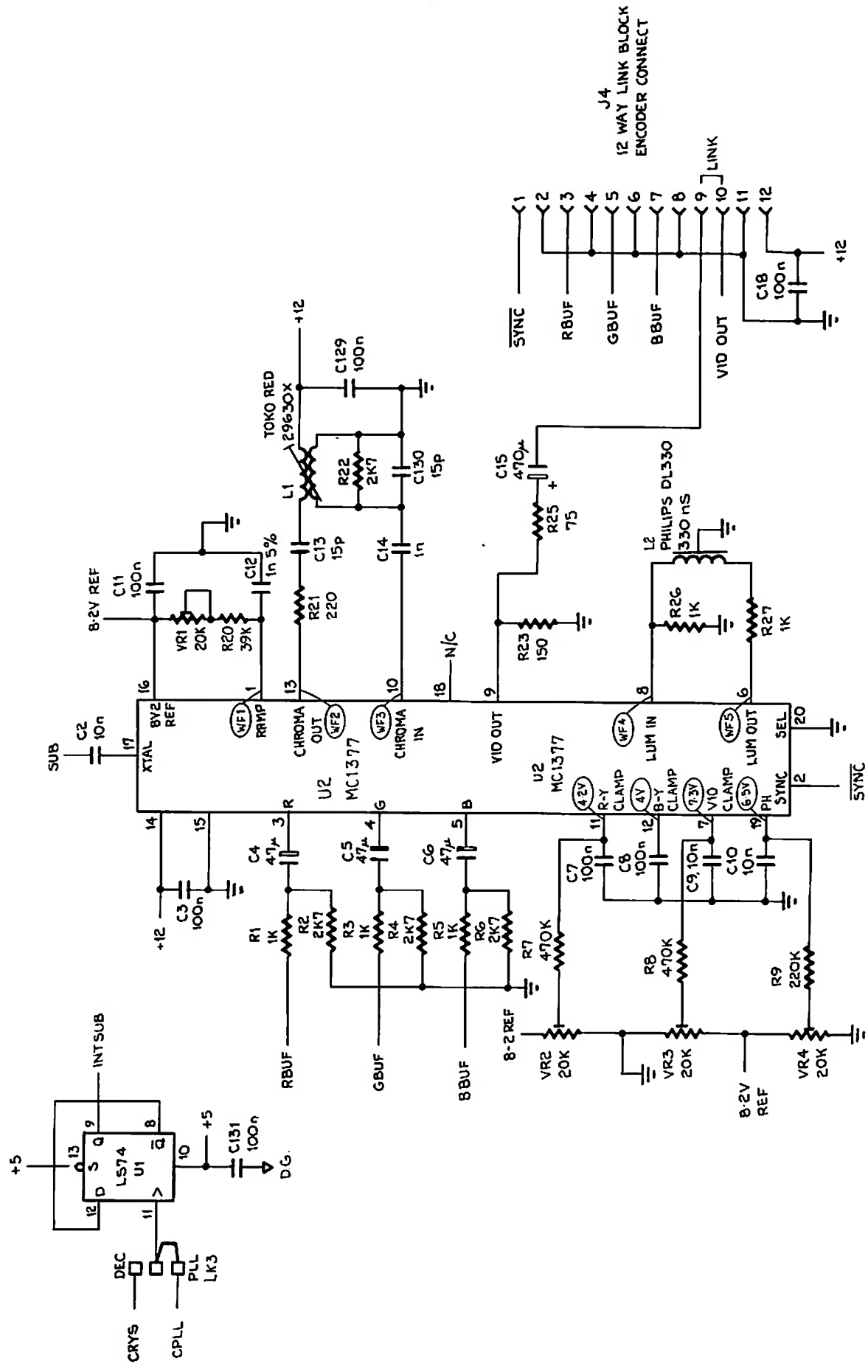
2) Loss of colour on composite input.
- Decoder XTAL OSC free run frequency wrong.
- Link LK4 or LK5 set in U position.
- Saturation controls set too low.

3) Screen tears and rolls.
- EXTSYNC signal is low when no input video to VIDEO 1.
- Vs or Hs signals are missing when in external sync.

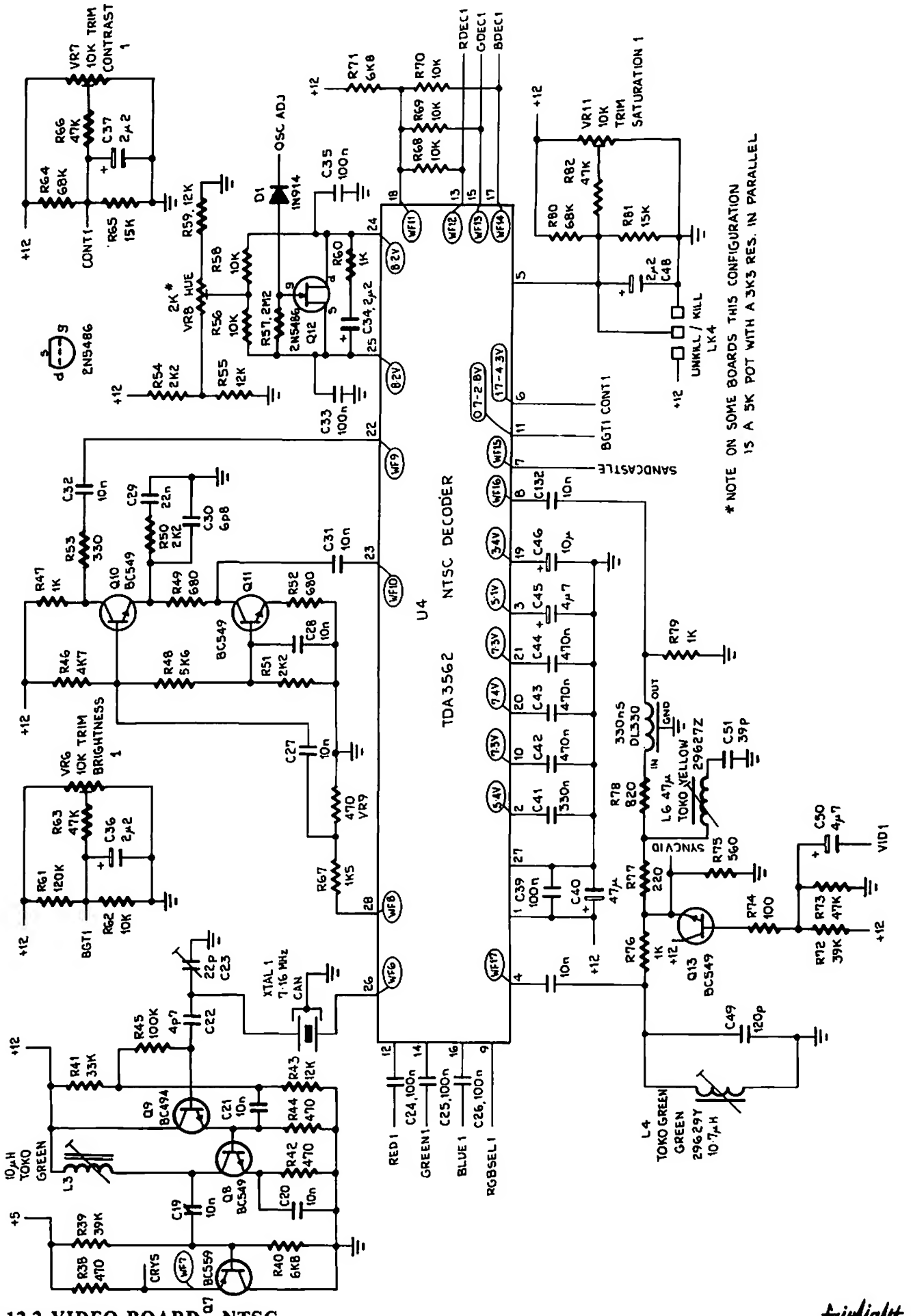
COMPONENT OVERLAY

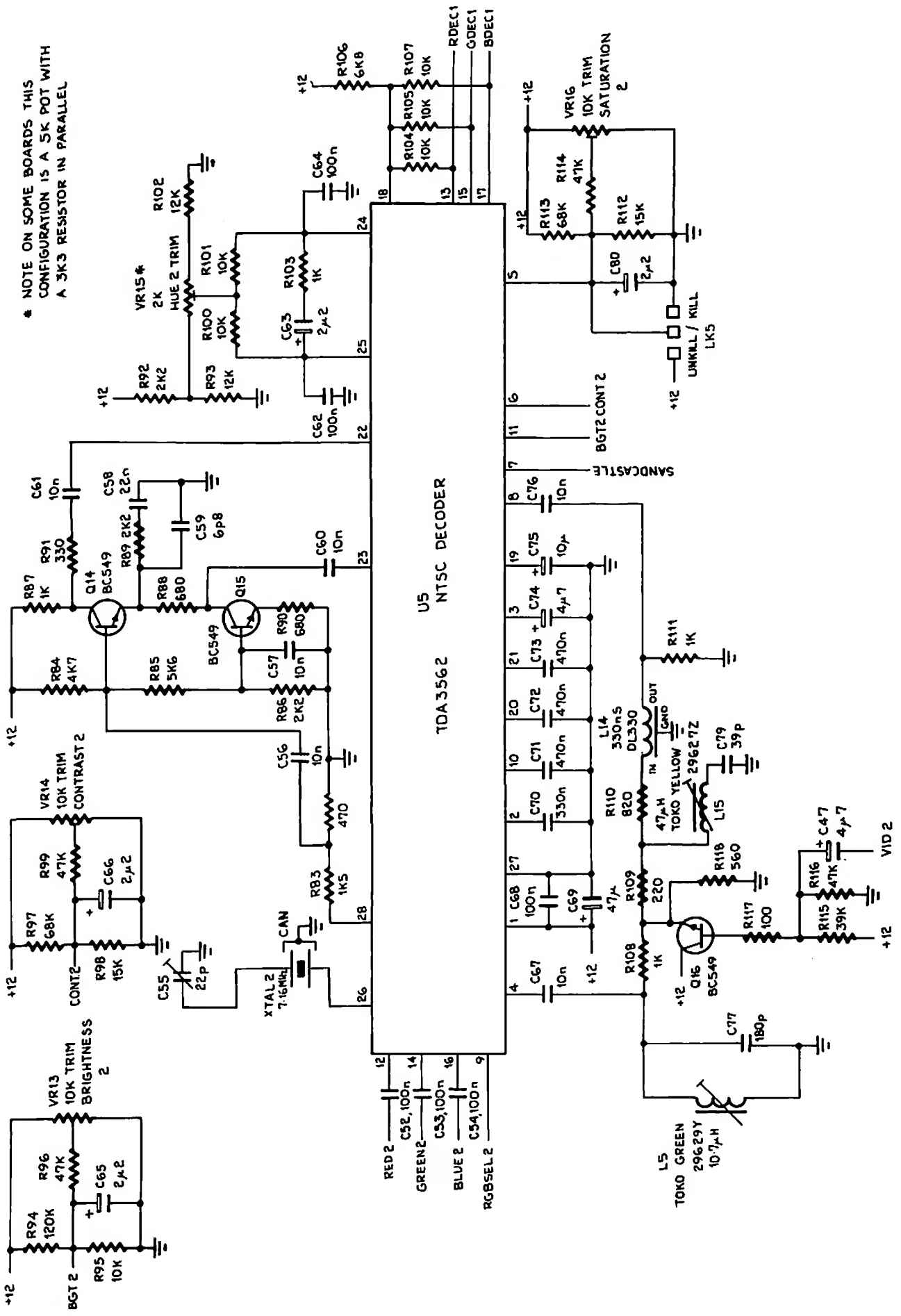



40 WAY HEADER TO BACK PANEL
1 GND
2 VIDEO 1 IN
3 GND
4 VIDEO 2 IN
5 GND
6 RED IN
7 GND
8 GREEN 1 IN
9 GND
10 BLUE 1 IN
11 GND
12 RED 2 IN
13 GND
14 GREEN 2 IN
15 GND
16 BLUE 2 IN
17 GND
18 STENCIL IN
19 GND
20 AUDIO IN
21 GND
22 SWITCH IN
23 GND
24 IN SUBCARRIER
25 GND
26 +12
27 GND
28 STENCIL OUT
29 GND
30 SYNC OUT
31 GND
32 RED OUT
33 GND
34 GREEN OUT
35 GND
36 BLUE OUT
37 GND
38 VIDEO OUT
39 GND
40 MIC OUT
MIC
VID OUT
R19 75
BBUF
R17 75
GBUF
R15 75
RBUF
R11 75
R10 560
Q1 BC549
SYNC
+12
R12 560
R13 75
Q2 BC549
STENCIL
+12
GAIN1
GAIN 2
RGBSEL1
RGBSEL2
SUBSEL
SUBPH1
SUBPH2
SW1
2x75
R37
R36
R35
R34
R33
R32
R31
5x3K3
+5
EXT SUB
+12
REMOTE
AUD
VID1
VID2
BLUE 2
GREEN 2
RED 2
BLUE 1
GREEN 1
RED 1
VID 2
VID 1
SW2
RP1
8x75
100n
LM311
U3
R30 10K
+5
R29 1K
-12
100n
DG
+12
+5
R28 1K
EXTM
OFF BOARD CONN.
VIDEO OUT
IN 2
IN 1
AUDIO
REMOTE
VIDOUT
VID2
VID1
MIC AUD
REMOTE
1 ASEL1
2 ASEL2
3 REMOTE
4 -12
5 +5
6 +12
7 EXTM
8 CRYS
9 STENCIL
10 CPLL
11 EXT SYNC
12 DRED
13 ARED
14 RBUF
15 DGREEN
16 AGREEN
17 GBUF
18 DBLUE
19 ABLUE
20 BBUF
21 SYNC
22 VS
23 HS
24 SBLANK
25 -5
26 BASS
27 MID
28 TREB
29 ENV
30 G
40 WAY HEADER TO MAIN BOARD

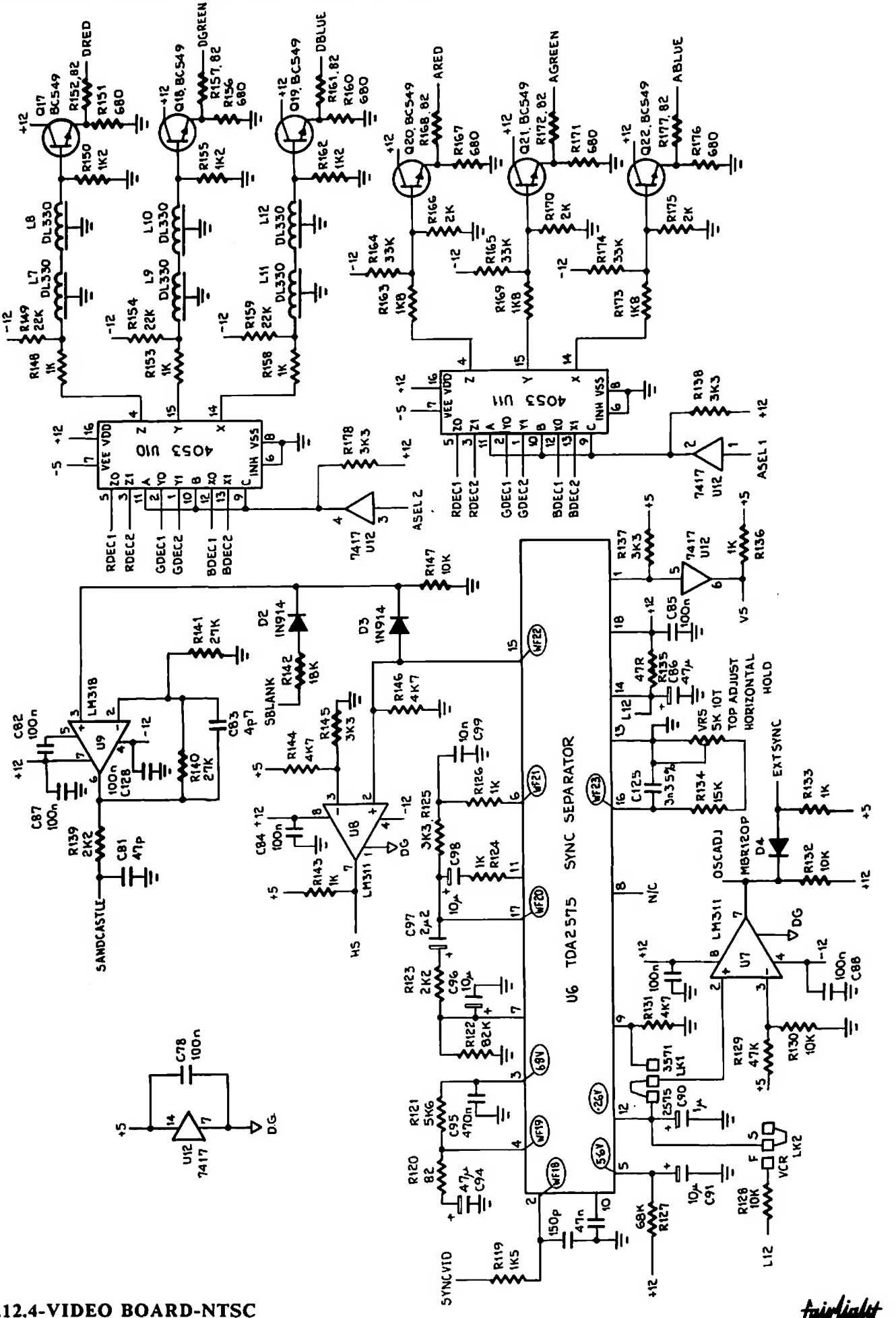

J4
12 WAY LINK BLOCK
ENCODER CONNECT
LINK
SYNC
RBUF
GBUF
BBUF
VID OUT
+12
C18 100n
C129 100n
TOKO RED 29630X
L1
R22 2K7
C130 15p
C13 15p
C14 1n
C15 470µ
R25 75
L2 PHILIPS DL330 330 nS
R26 1K
R27 1K
R23 150
8·2V REF
C11 100n
C12 1n 5%
VR1 20K
R20 39K
R21 220
N/C
C2 10n
SUB
XTAL
BY2 REF
WF1 RAMP
CHROMA OUT
WF2
WF3 CHROMA IN
VID OUT
WF4 LUM IN
WF5 LUM OUT
SEL
U2 MC1377
4·2V R-Y CLAMP
4V B-Y CLAMP
1·3V V10 CLAMP
6·5V PH SYNC
C3 100n
C4 47µ
C5 47µ
C6 47µ
R1 1K
R2 2K7
R3 1K
R4 2K7
R5 1K
R6 2K7
C7 100n
C8 100n
C9 10n
C10 10n
R7 470K
R8 470K
R9 220K
VR2 20K
VR3 20K
VR4 20K
INTSUB
L574 U1
C131 100n
DEC
PLL LK3
CRYS
CPLL
D.G.

DECODER FOR VIDEO 1 INPUT



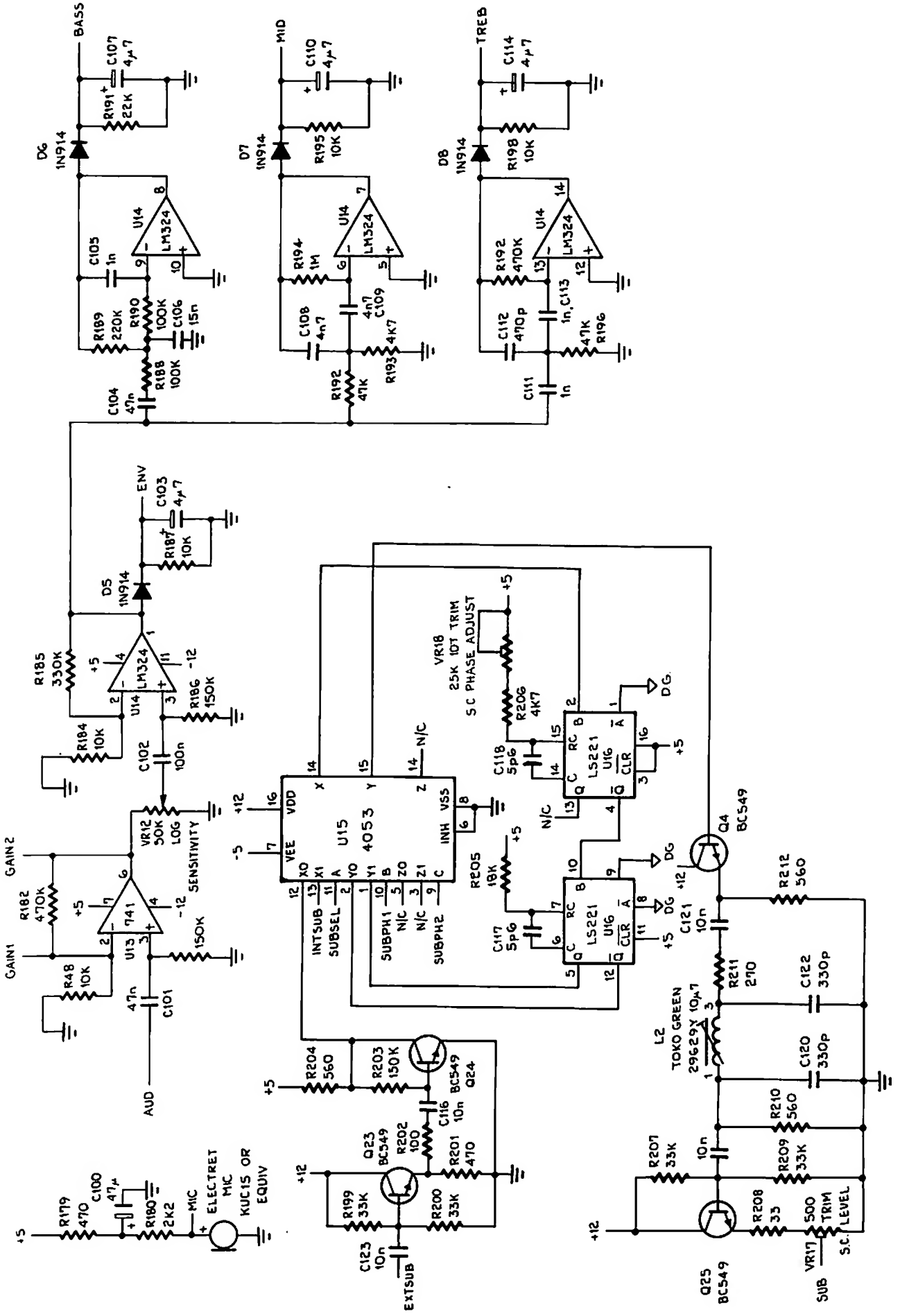

* NOTE ON SOME BOARDS THIS CONFIGURATION IS A 5K POT WITH A 3K3 RESISTOR IN PARALLEL
U5 NTSC DECODER TDA3562
VR15* 2K HUE 2 TRIM
VR16 10K TRIM SATURATION 2
VR14 10K TRIM CONTRAST 2
VR13 10K TRIM BRIGHTNESS 2
BGT2 CONT 2
SANDCASTLE
UNKILL / KILL LK5
XTAL 2 7.16MHz
CAN
RED 2
GREEN 2
BLUE 2
RGBSEL 2
RDEC1
GDEC1
BDEC1
VID 2
L14 330nS DL330
L15 47µH TOKO YELLOW 296272
L5 TOKO GREEN 29629Y 10·7µH
Q14 BC549
Q15 BC549
Q16 BC549
CONT2
+12

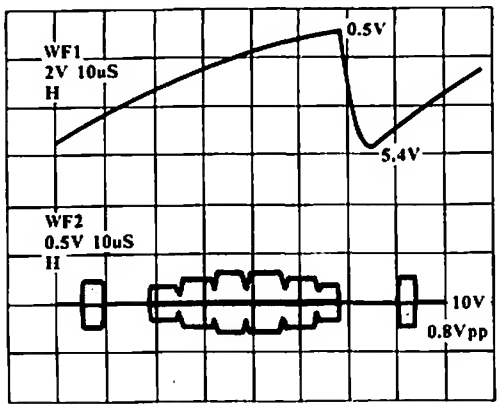
SYNC SEPARATOR FOR VIDEO MULTIPLEXER

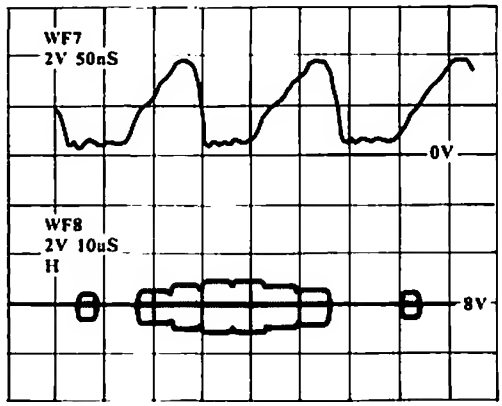


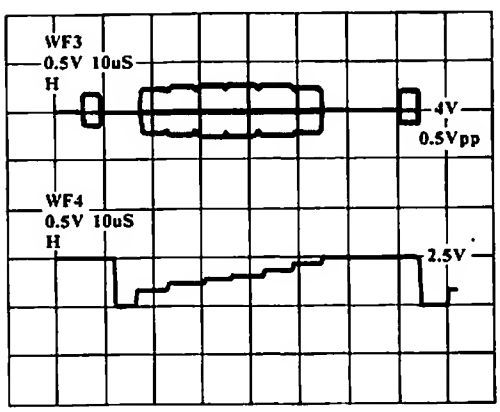
fairlight

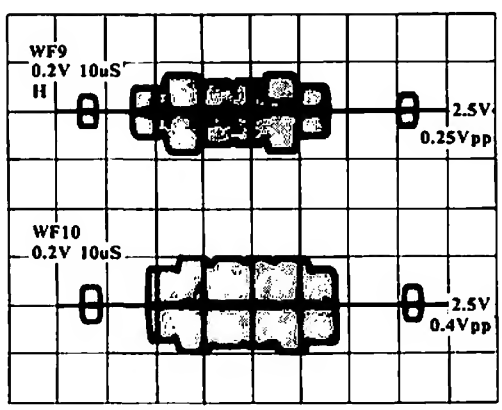
AUDIO INPUT AND FILTERS + SUBCARRIER PHASE ADJUST

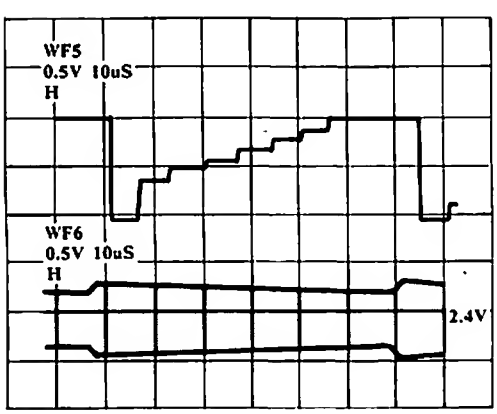


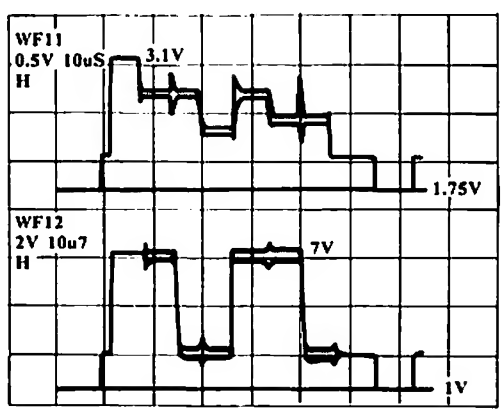

WF1
2V 10uS
H
0.5V
5.4V
WF2
0.5V 10uS
H
10V
0.8Vpp

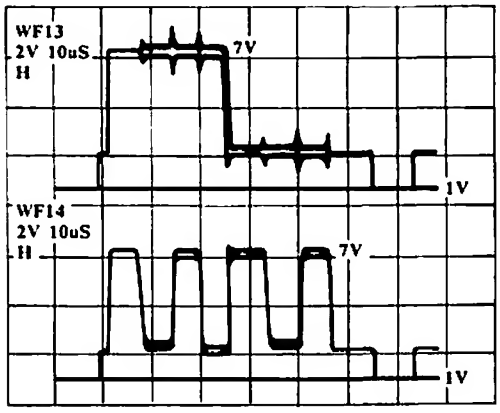

WF7
2V 50nS
0V
WF8
2V 10uS
H
8V

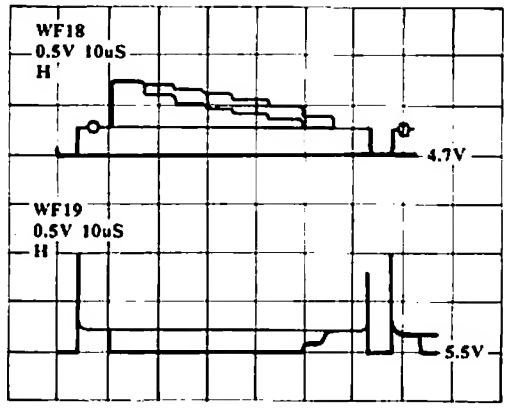

WF3
0.5V 10uS
H
4V
0.5Vpp
WF4
0.5V 10uS
H
2.5V

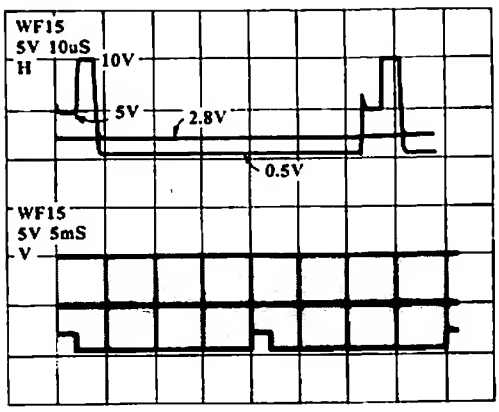

WF9
0.2V 10uS
H
2.5V
0.25Vpp
WF10
0.2V 10uS
2.5V
0.4Vpp

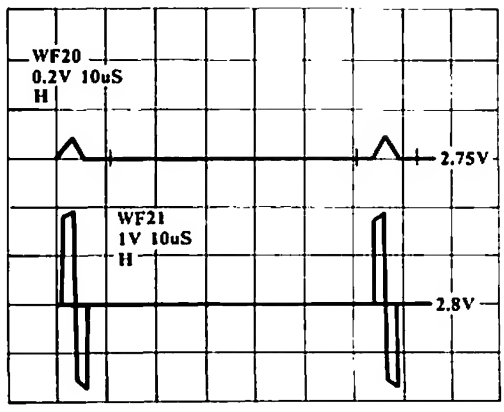

WF5
0.5V 10uS
H
WF6
0.5V 10uS
H
2.4V

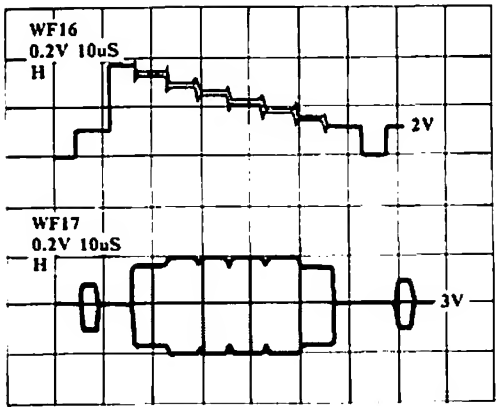

WF11
0.5V 10uS
H
3.1V
1.75V
WF12
2V 10u7
H
7V
1V

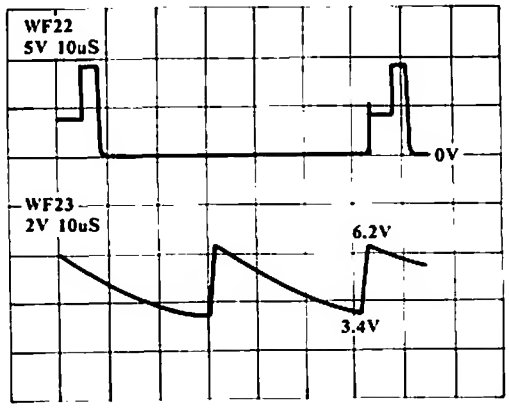

WF13
2V 10uS
H
7V
1V
WF14
2V 10uS
H
7V
1V


WF18
0.5V 10uS
H
4.7V
WF19
0.5V 10uS
H
5.5V

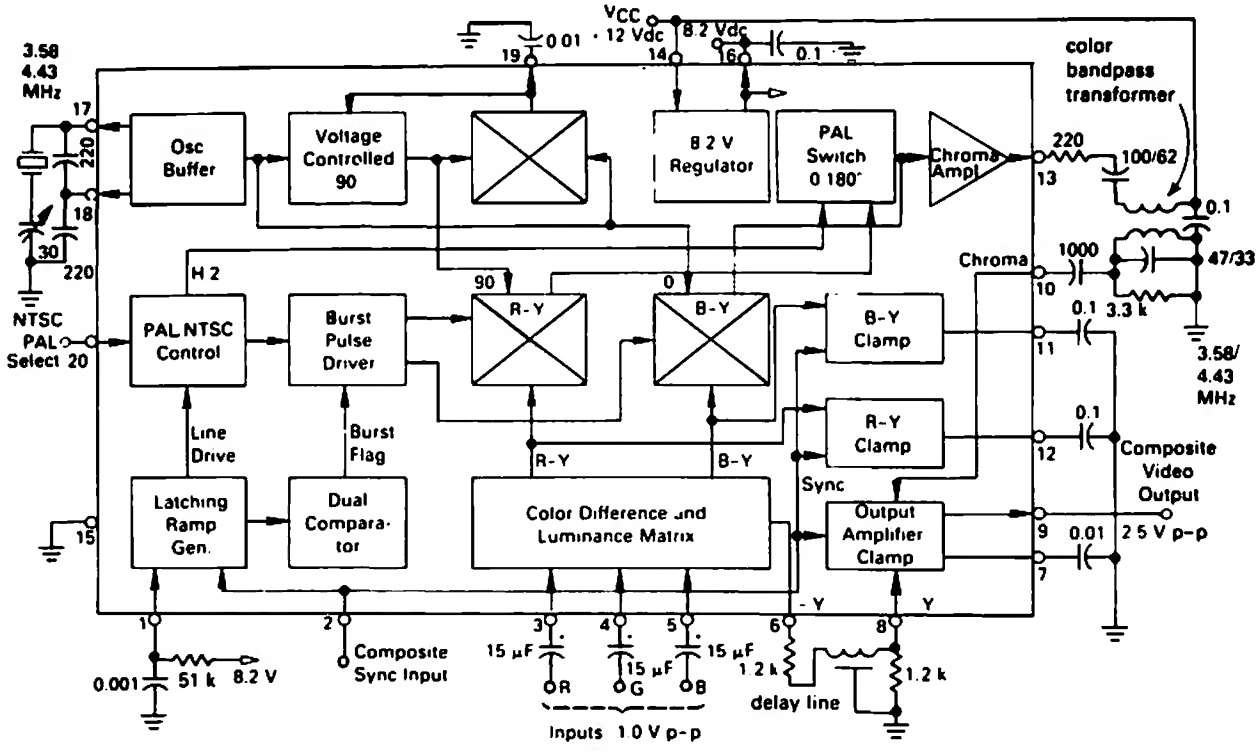

WF15
5V 10uS
H
10V
5V
2.8V
0.5V
WF15
5V 5mS
V


WF20
0.2V 10uS
H
2.75V
WF21
1V 10uS
H
2.8V

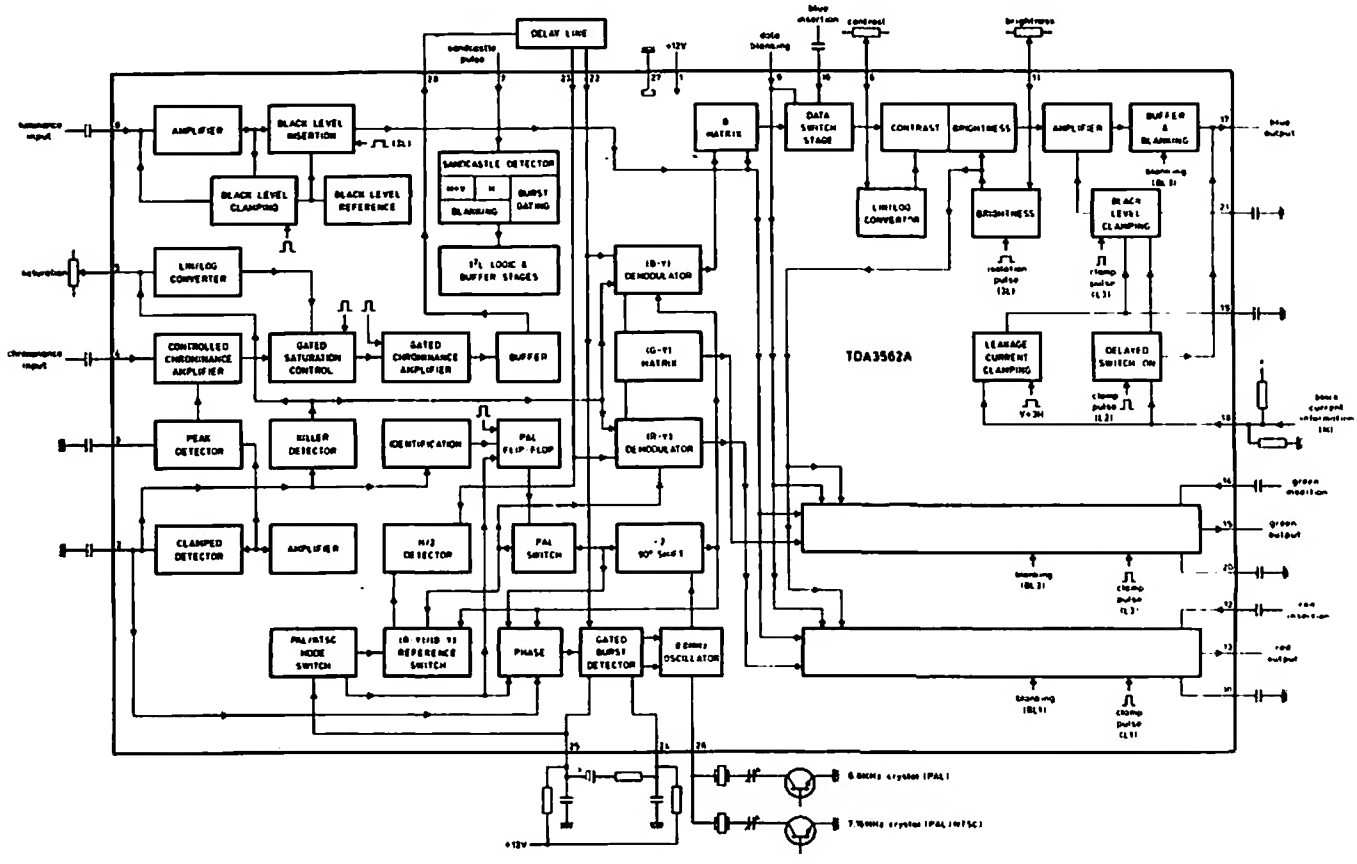

WF16
0.2V 10uS
H
2V
WF17
0.2V 10uS
H
3V


WF22
5V 10uS
0V
WF23
2V 10uS
6.2V
3.4V

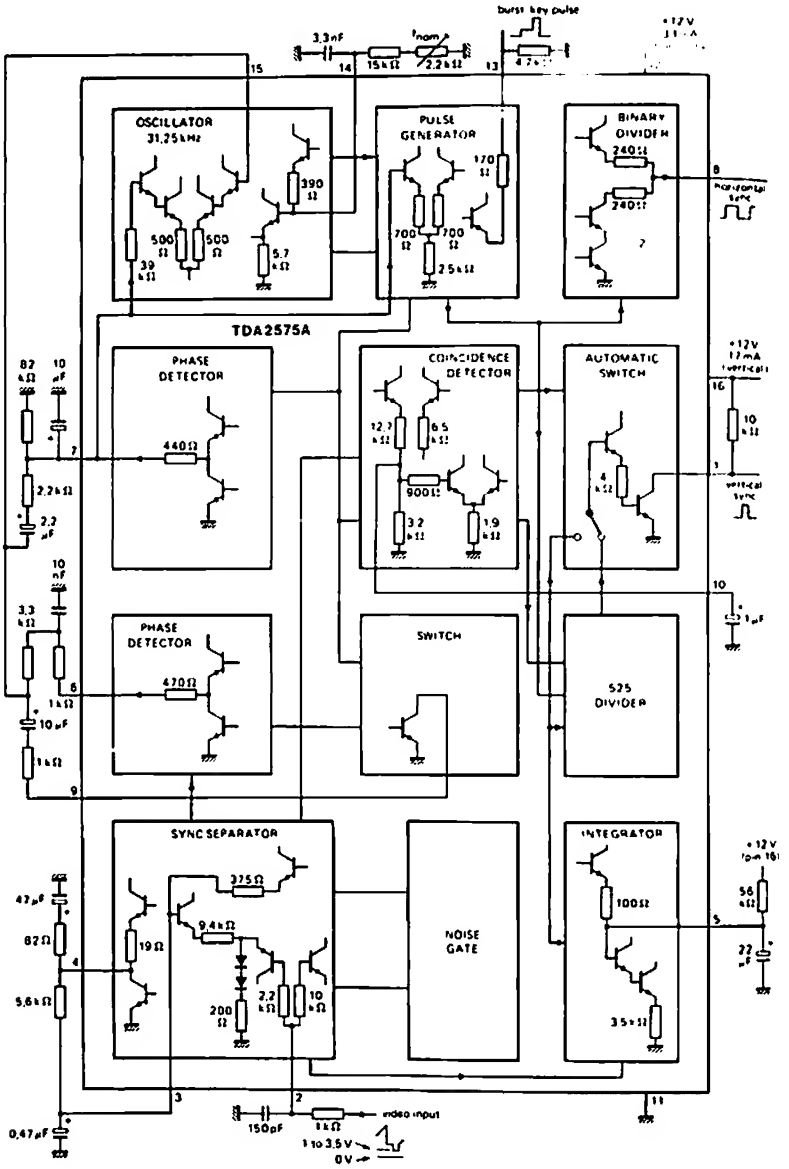
MC 1377P ENCODER



TDA 3562A DECODER



fairlight


TDA2575A
OSCILLATOR
31.25kHz
PULSE GENERATOR
BINARY DIVIDER
PHASE DETECTOR
COINCIDENCE DETECTOR
AUTOMATIC SWITCH
PHASE DETECTOR
SWITCH
525 DIVIDER
SYNC SEPARATOR
NOISE GATE
INTEGRATOR
burst key pulse
video input
horizontal sync
vertical sync

General

The CVI-08N sync board when installed in place of the TDA2575 chip on CVI-03N rev4 and rev4x NTSC video boards provides improved syncing especially to video tape signals. It provides faster lockup to unstable video input signals due to a shorter time constant.

Circuit Description

The lowpass filtered video signal from U6 pin 2 on CVI-03N is buffered by Q1 and sync tip clamped by comparator U3B to a level determined by zener diode D2. Composite sync is separated by comparator U1. Half line information is deleted by monostable U2B and the resultant line rate signal is buffered by Q2 and fed to the sync processor U4 pin 1. The separated sync from U1 pin 7 is integrated at the input to monostable U2A to derive a vertical sync signal at U2A pin 13 which is also fed to the sync processor U4 pin 24.

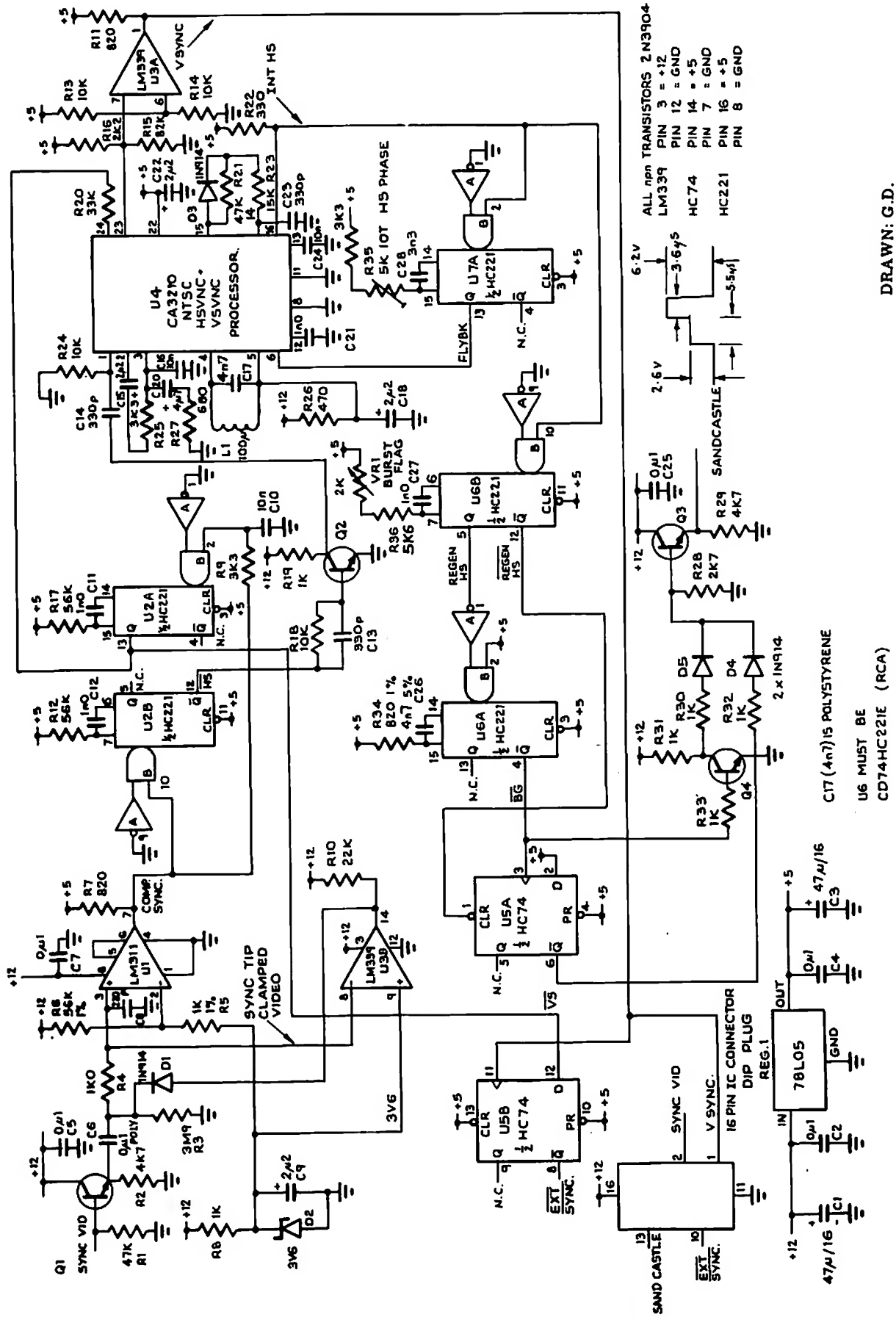
The sync processor U4 regenerates the horizontal signal from a phase locked loop. The time constant for this loop is controlled by components connected to pins 2 and 3. The oscillator frequency is controlled by components connected to pins 4 and 5. The regenerated vertical signal is derived from an internal counter when a standard video signal (525 lines) is connected. When non-standard signals are connected the vertical signal is derived directly from the separated signal to U4 pin 24.

Processed vertical sync at U4 pin 23 is detected by comparator U3A. This signal is used as vertical reset on the CVI-01 board when in external sync mode. Flip-flop U5B samples the separated vertical sync signal from U2A pin 13 on the rising edge of the processed vertical sync signal from U3A pin 1 and provides a low signal at U5B pin 8 if there is coincidence indicating external lock. This signal is used on the CVI-01 board to select external sync mode.

The horizontal drive output from U4 pin 16 is delayed by monostable U7a to provide a flyback signal required by U4 for correct phasing of the incoming and processed horizontal sync signals. The start of the burst gate signal is determined by VR1 and U6B which is triggered on the rising edge of the horizontal drive from U4. The burst gate length is set by monostable U6A, R34 and C26.

The multilevel "sandcastle" signal required by the decoders is generated by U5A, Q3 and Q4. The highest level occurs during the burst period and is generated by Q4. The middle level indicates the horizontal sync period and is generated by U5A pin 6, R32 and D4. The resulting signal is buffered by Q3.

The +12v supply is smoothed by capacitor C1. The +5v supply is derived from +12v by REG1 and smoothed by C3 and C4.


ALL npn TRANSISTORS 2N3904
LM339 PIN 3 = +12
PIN 12 = GND
HC74 PIN 14 = +5
PIN 7 = GND
HC221 PIN 16 = +5
PIN 8 = GND
DRAWN: G.D.
U4 CA3210 NTSC HSYNC+ VSYNC PROCESSOR
VSYNC
INT HS
HS PHASE
FLYBK
BURST FLAG
SANDCASTLE
REGEN HS
COMP. SYNC.
SYNC TIP CLAMPED VIDEO
SYNC VID
SAND CASTLE
EXT SYNC.
V SYNC.
16 PIN IC CONNECTOR DIP PLUG
REG.1
78L05
C17 (4n7) IS POLYSTYRENE
U6 MUST BE CD74HC221E (RCA)

Equipment

- oscilloscope 100MHz, dual channel
- video test signal generator (NTSC)
- video cassette recorder (NTSC)
- CVI (NTSC), tested and calibrated

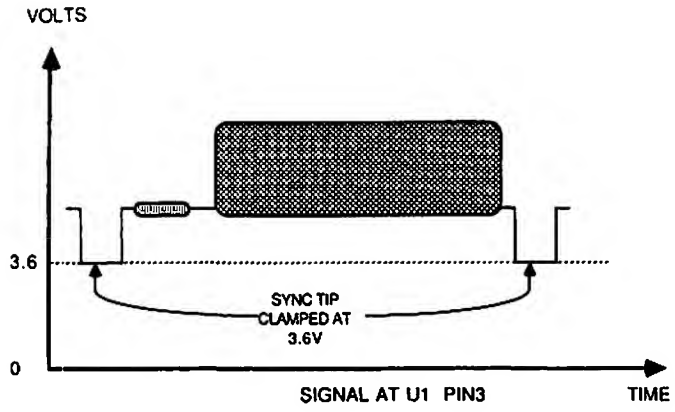
Setup

- Connect video signal generator to VIDEO 1 input.
- CRO CH1 connected to input video signal trigger on CH1

Procedure

1) Connect an NTSC video signal to the VIDEO 1 input.

2) Check that the input video sync tip at U1 pin3 is clamped to about 3v6 as set by D2. See figure below.



3) Check for separated sync on U1 pin 7 at TTL levels.

4) Check that the leading edge of the signal on U2 pin 13 occurs during the first line of the vertical sync period of the input video.

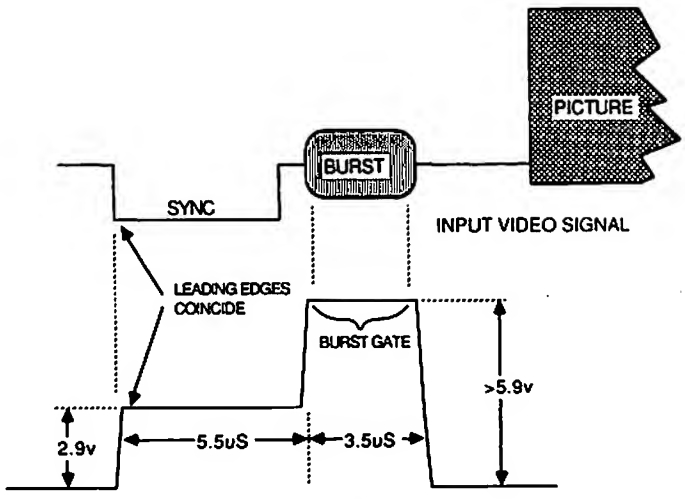
5) Check that the EXTSYNC signal (U5 pin 8) is at zero volts when an external video signal is connected to VIDEO 1 input and is greater than 3 volts when the input to VIDEO 1 is disconnected.

6) Adjust VR2/R35 (5k trimpot) so that the leading edge of the sandcastle signal at emitter of Q3 is in phase with the horizontal sync of the input video. See figure below.

7) Adjust VR 1 so that the sandcastle burst gate coincides with the input burst. See figure below.

8) Check that the sandcastle signal has approximately correct durations and levels. See figure below.

9) Check that the CVI-08N board locks to the VCR off-tape signal without tearing at the top of the screen or excessive instability.

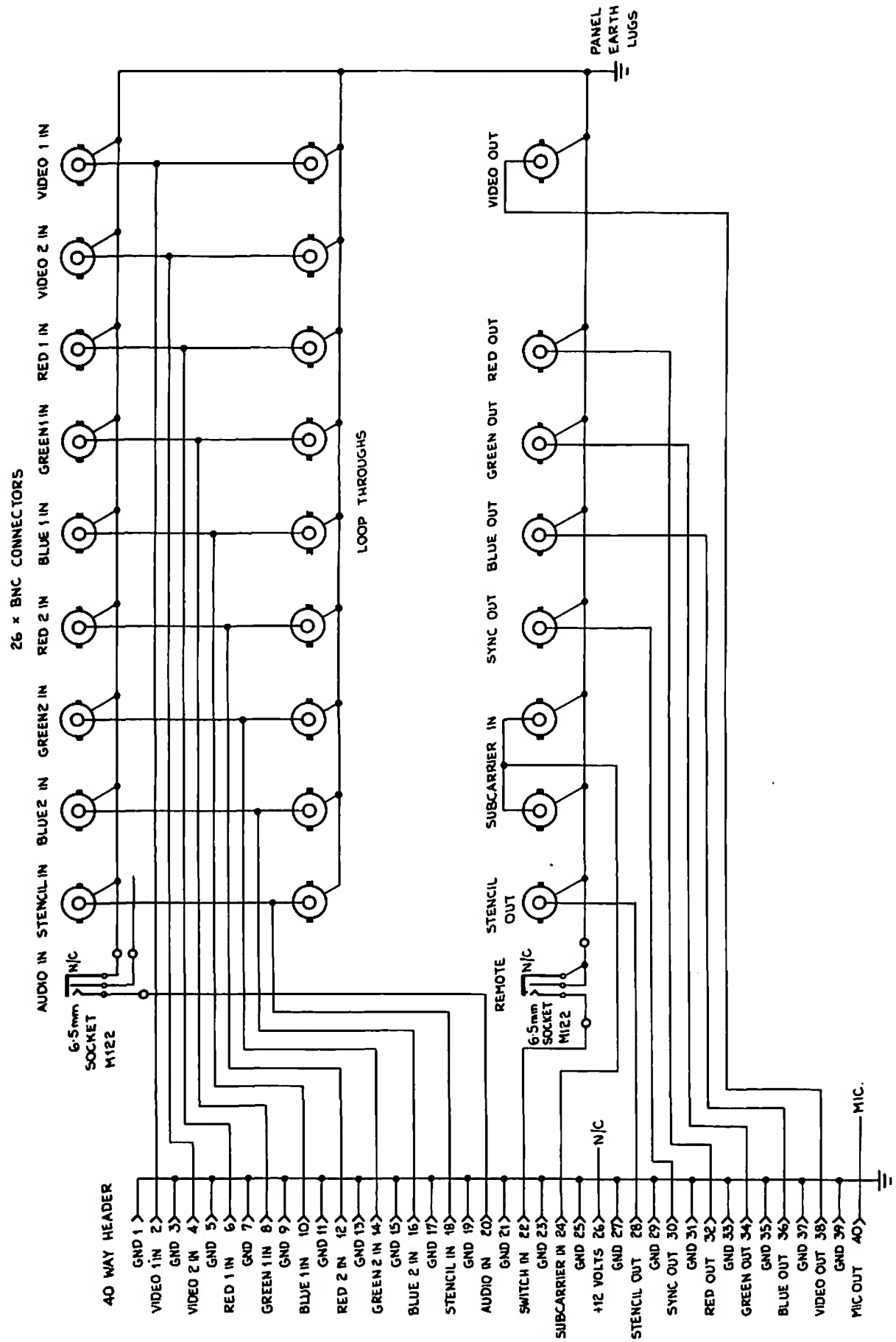


SANDCASTLE SIGNAL AT EMITTER Q3

BNC Connector Board 5

CONTENTS

BNC CONNECTOR DIAGRAM



Power Supply 6

CONTENTS

FUSE REPLACEMENT

WARNING

Fuse replacement should be undertaken only by experienced personnel. FAIRLIGHT INSTRUMENTS is not liable for any damage due to improper installation. Should you be unsure of the installation procedure we recommend that you consult Fairlight Instruments, your distributor or qualified service personnel.

1. Turn the unit off and unplug the mains cable.
2. Remove the facia panel from the unit and slide out the tray.
3. Undo the four screws that secure the cover of the power supply. Remove and retain the four screws and their locking washers
4. Lift the power supply away from the main tray, avoiding strain on the flat connector cable.
5. Remove the fuse from its socket in the power supply.
6. If the fuse is blown, replace it with a new fuse of the same size and rating (2A, 250V).
7. Place the power supply unit on the main tray. Avoid twisting or straining the flat connector cable. The orange button should face the front of the tray.
8. Replace the four screws, each with a locking washer. Do not over-tighten.
9. Slide the tray back into the case and replace the facia panel.
10. Plug in the mains cable and turn the unit on. The normal start-up sequence should follow.

If the CVI fails to start up correctly:

1. Check that the power cable is plugged in.
2. Unplug the power cable and follow steps 1-10 again, checking all connections.
3. If the unit still does not start, contact your distributor.

WARNING

Change of the supply voltage should be undertaken only by experienced personnel. FAIRLIGHT INSTRUMENTS is not liable for any damage due to improper voltage settings. Should you be unsure of the procedure or of the local supply voltage we recommend that you consult Fairlight Instruments, your distributor or qualified service personnel.

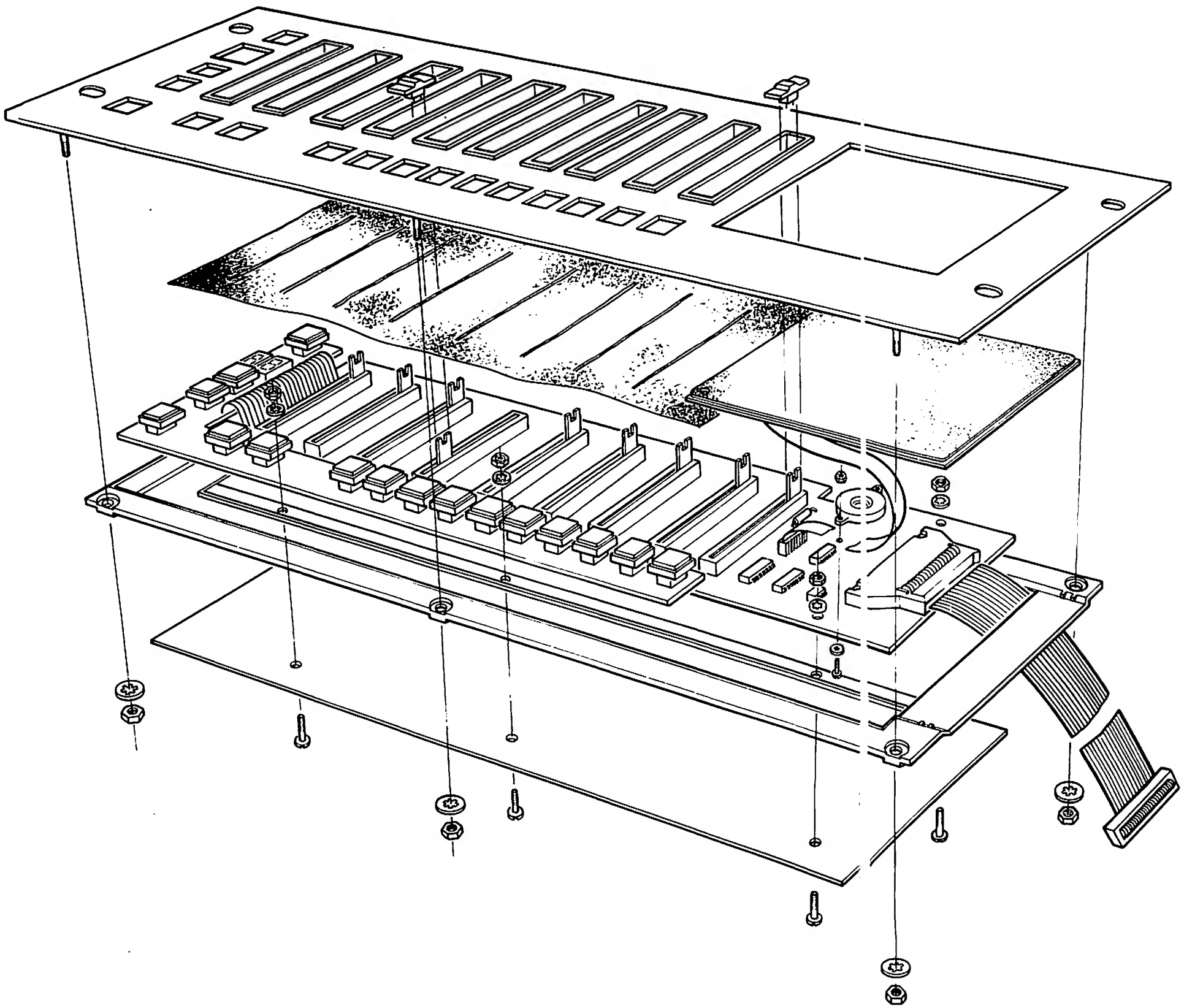
1. Turn the unit off and unplug the mains cable.
2. Remove the facia panel from the unit and slide out the tray.
3. Undo the four screws that secure the cover of the power supply. Remove and retain the four screws and their locking washers
4. Lift the power supply away from the main tray, avoiding strain on the flat connector cable.
5. Remove the black link marked "SEL" from its lug.
6. Place the "SEL" link firmly on the lug marked with the local supply voltage (i.e. either on "230" for 200-240V AC or on "115" for 100-120V AC).
7. Change the voltage indication on the back of the rack unit to the new setting. This marking is immediately below the power socket on the back of the CVI.
8. Place the power supply unit on the main tray. Avoid twisting or straining the flat connector cable. The orange button should face the front of the tray.
9. Replace the four screws, each with a locking washer. Do not over-tighten.
10. Slide the tray back into the case. Replace the facia panel
11. Plug in the mains cable and turn the unit on. The normal start-up sequence should follow.

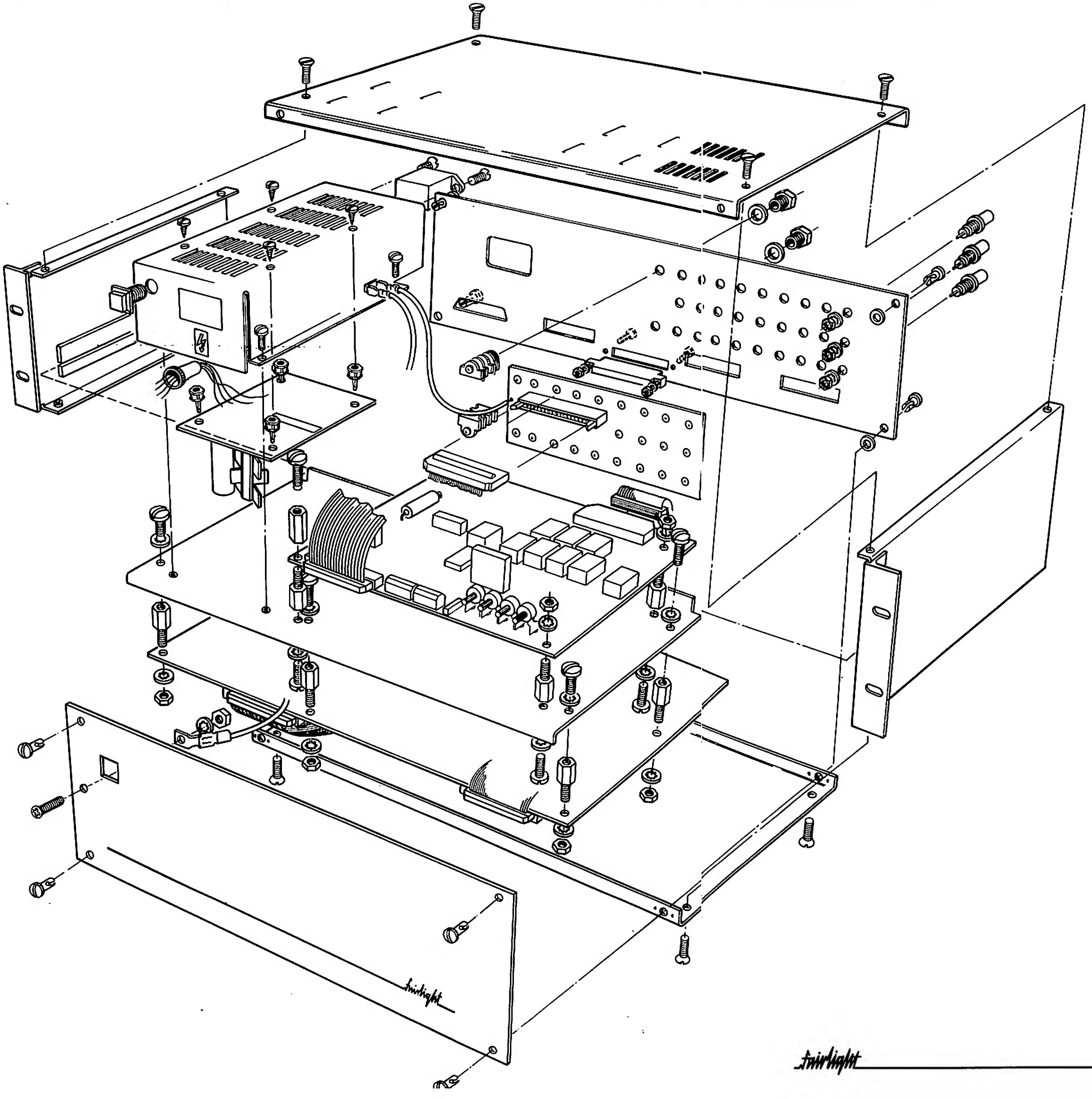
If the CVI fails to start up correctly:

1. Check that the power cable is plugged in.
2. Unplug the power cable and follow steps 1-11 again, checking all connections.
3. If the unit still does not start, contact your distributor.

Exploded Diagrams 7

CONTENTS





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Fairlight Instruments Pty Ltd,
15-19 Boundary Street,
Rushcutters Bay, NSW, 2011,
AUSTRALIA.

Phone: (02) 331 6333
Telex: 27998 'FAIRLT'
Fax: (02) 332 3362

SERVICE CENTRES

U.S.A.
Fairlight Instruments Inc.,
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28040 Varallo, Pombia (NO),
Piemonte, Italy.
Phone: 0321 956754
Telex: 200203 'CEMEL I'

WEST GERMANY
FSG-Fernseh-System-VertriebsGmbH,
Sonnenstrasse 5,
D-8042 Obershleissheim-Muenchen,
Germany.
Phone:
Telex: 5215406 'FSG D'

Elmulab,
Bergstraesserstrasse 7,
8000 Munchen 50,
Germany.
Phone: (089) 812 0574
Telex: 17898385 'NETZLE TTXD'

FRANCE
Studio de la Frette,
10 Rue Jean Lefebure,
La Frette sur Seine,
95530, Paris, France.
Phone: (4) 347 4664
(3) 978 5161
Telex: 211184 'AUDITIF'

BENELUX
Synton Electronics B.V.,
Postbus 83,
3620 AB Breukelen, Holland.
Phone: (03462) 63499
Telex: 40541 'SYNTO NL'

Synton Electromusic PVBA,
57-59 Avenue de Stalingrad,
B-1000 Brussels, Belgium.
Phone: (02) 512 0574

DENMARK
SLT,
Helgesvej, 7-13,
2000 Copenhagen F,
Denmark.
Phone: (01) 34 1284
Telex: 22942 'SLT DK'

FINLAND
Studio Tec,
Sininarhentie 5,
SF-02600,
ESPOO 60, Finland.
Phone: 90 514133
Telex: 125281 'STUTE SF'